

# Discrete/UMA Schematics Document

## Sandy Bridge

### Intel PCH

#### 2011-01-04

#### REV : A00

*DY :None Installed*

*UMA:UMA ONLY installed*

*DN15: ONLY FOR DN15 installed.*

*DQ15:ONLY FOR DQ15 installed.*

*PSL: KBC795 PSL circuit for 10mW solution installed.*

*10mW: External circuit for 10mW solution installed.*

*MUXLESS:MUXLESS solution installed.*

*OPTIMUS:OPTIMUS solution installed.*

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A3

Document Number

**QUEEN 15**

Rev

**A00**

Date: Tuesday, January 04, 2011

Sheet 1 of 108

# Block Diagram (Discrete/UMA co-lay)

SYSTEM LDO APL5916 48		CPU DC/DC ISL95831HRTZ 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_VTT	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC TPS51311 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9731 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

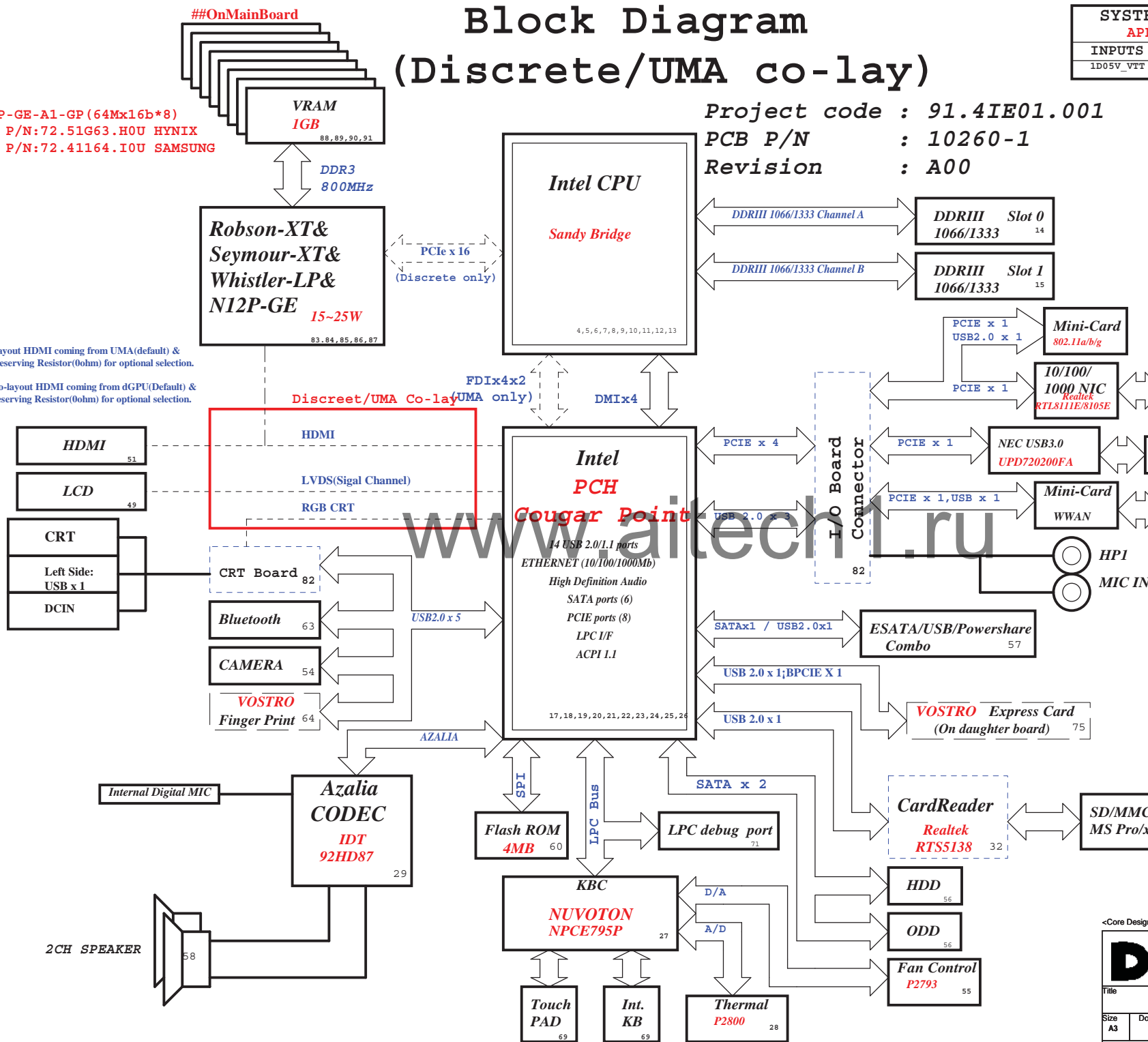
PCB LAYER	
L1:Top L2:VCC L3:Signal	L4:Signal L5:GND L6:Bottom

##OnMainBoard

1.N12P-GE-A1-GP (64Mx16b\*8)  
WKS P/N:72.51G63.H0U HYNIX  
WKS P/N:72.41164.I0U SAMSUNG

ATI : Co-layout HDMI coming from UMA(default) &  
dGPU by reserving Resistor(0ohm) for optional selection.

NVidia : Co-layout HDMI coming from dGPU(Default) &  
UMA by reserving Resistor(0ohm) for optional selection.



<Core Design>

**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title **Block Diagram**

Size A3 Document Number **QUEEN 15** Rev **A00**

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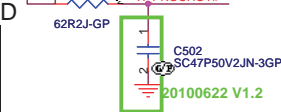


[illegible]



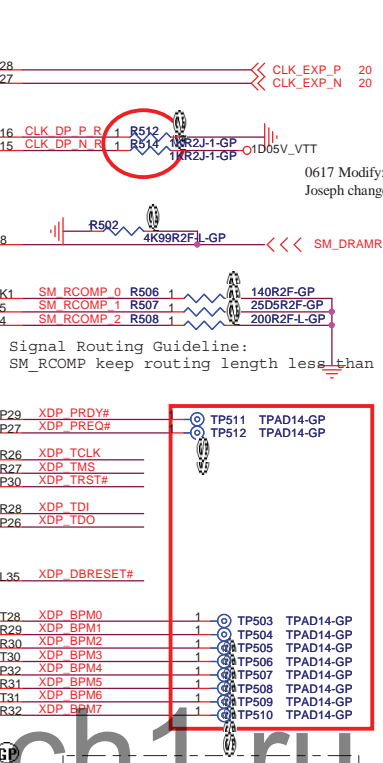
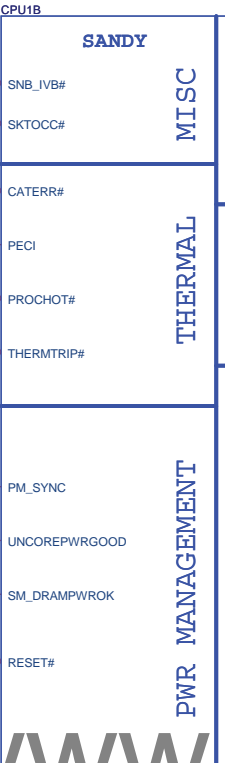
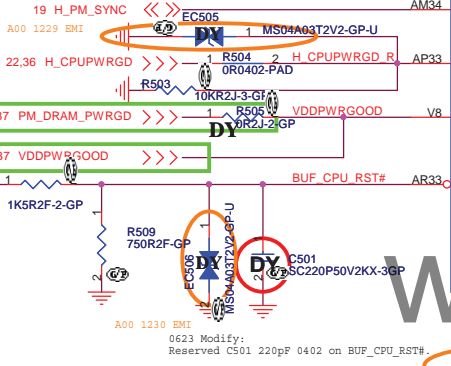
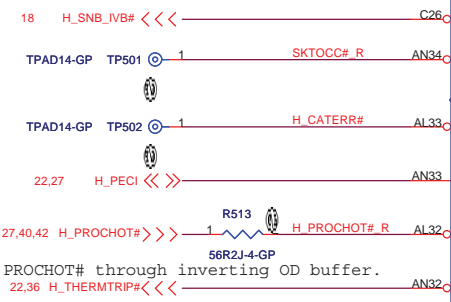
SSID = CPU

0625 Modify:  
Add C502 47pF 0402 on H\_PROCHOT#.



CRB : 47pF  
CEKLT: 43pF

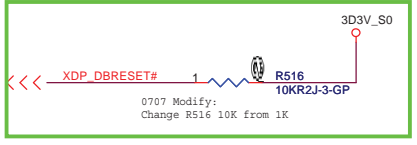
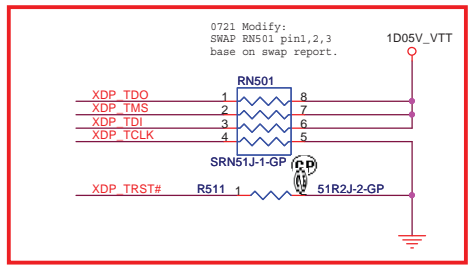
Connect EC to PROCHOT# through inverting OD buffer.



Disabling Guidelines:  
If motherboard only supports external graphics:  
Connect DPLL\_REF\_SSCLK on Processor to GND through  
1K +/- 5% resistor.  
Connect DPLL\_REF\_SSCLK# on Processor to VCCP  
through 1K +/- 5% resistor power (~15 mW) may be  
wasted.

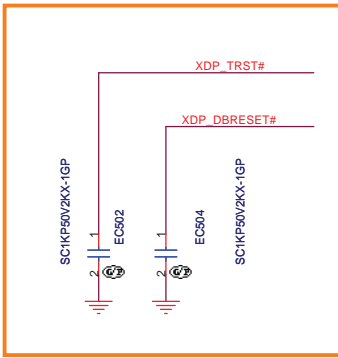
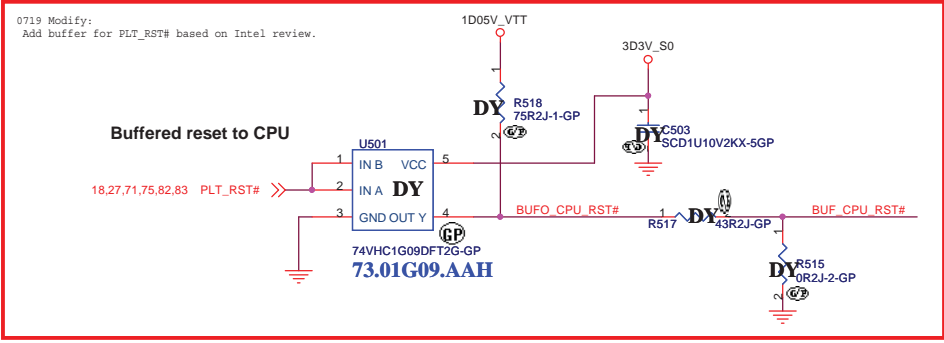
0617 Modify:  
Joseph change RN501 to R512, R514 1K 0402 Resistor.

Signal Routing Guideline:  
SM\_RCOMP keep routing length less than 500 mils.



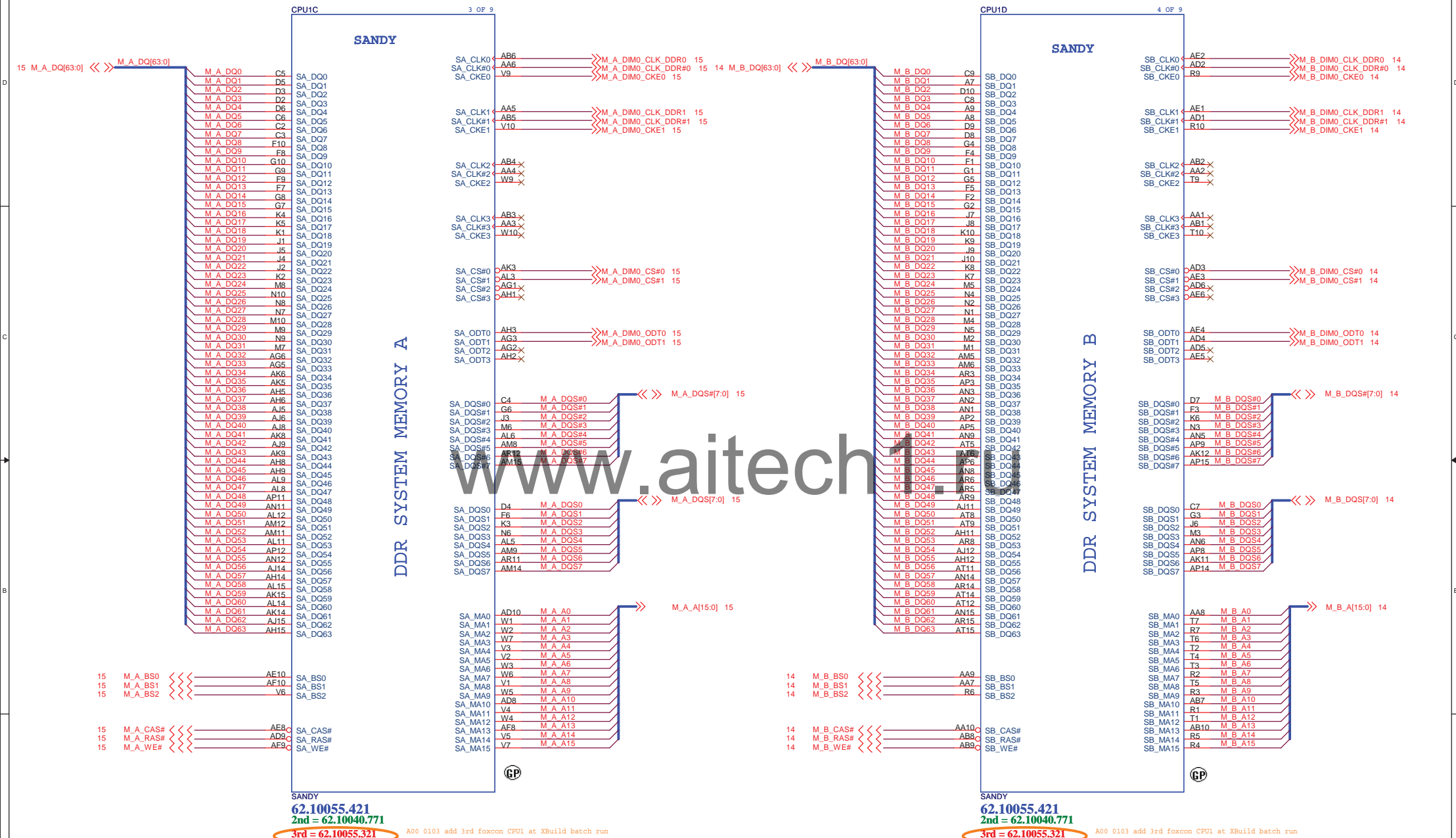
0630 Modify:  
Removed XDP110T connector  
related circuit by layout limitation.

0617 Modify:  
Joseph Removed U501 Buffer reset to CPU circuit.



A00 1229 EMI

SSID = CPU



SANDY  
62.10055.421  
2nd = 62.10040.771  
3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

SANDY  
62.10055.421  
2nd = 62.10040.771  
3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

<Variant Name>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>CPU (DDR)</b>		
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
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SSID = CPU

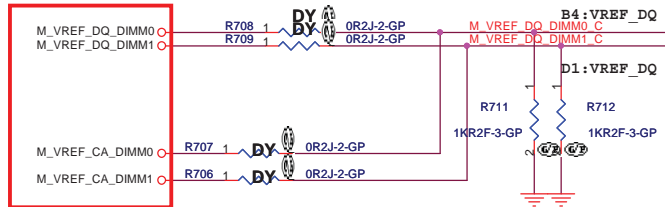
0630 Modify:  
Reserved TP715 on CFG0.

TPAD14-GP TP715

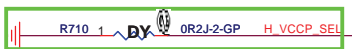
0707 Modify:  
Removed CFG1,CFG3,CFG8-17 TP.

0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0,M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0,M\_VREF\_CA\_DIMM1  
from net to power.

### M3 - Processor Generated SO-DIMM VREF\_DQ



0629 Modify:  
Reserved R710 0ohm to GND to  
follow EV board schematic.



1D05V\_VTT



0719 Modify:  
Reserved EC701 0.1uF near  
R711(BOTTOM) for EMC NEO suggestion.

CPU1E

5 OF 9

SANDY

RESERVED

SANDY SKT-BGA989C470395-1H180

62.10055.421

2nd = 62.10040.771

3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

RSVD#L7  
RSVD#AG7  
RSVD#AE7  
RSVD#AK2  
RSVD#W8

RSVD#AT26  
RSVD#AM33  
RSVD#AJ27

RSVD#T8  
RSVD#J16  
RSVD#H16  
RSVD#G16

RSVD#AR35  
RSVD#AT34  
RSVD#AT33  
RSVD#AP35  
RSVD#AR34

RSVD#B34  
RSVD#A33  
RSVD#A34  
RSVD#B35  
RSVD#C35

RSVD#AJ32  
RSVD#AK32

RSVD#AH27

RSVD#B30  
RSVD#B29  
RSVD#B31  
RSVD#B30  
RSVD#B31

RSVD#AT2  
RSVD#AT1  
RSVD#AR1

GP

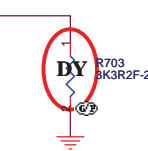
CFG2



#### PEG Static Lane Reversal

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	---

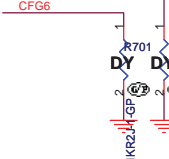
CFG4



#### Display Port Presence Strap

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

CFG5  
CFG6



#### PCIe Port Bifurcation Straps

CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled
----------	--

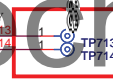
CFG7



#### PEG DEPER TRAINING

CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

0702 Modify:  
AN35 TP713  
AM35 TP714



0630 Modify:  
Removed CFE\_XDP\_VDD\_P01  
and reserved TP713,TP714.

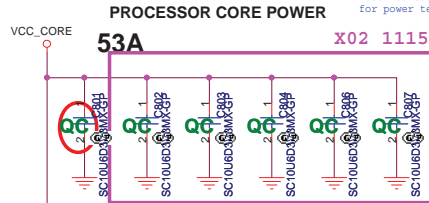
<Variant Name>

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
File <b>CPU (RESERVED)</b>			
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>	
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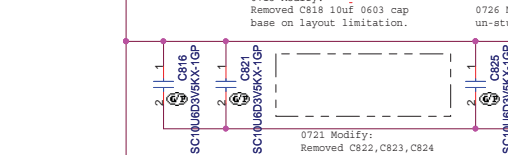
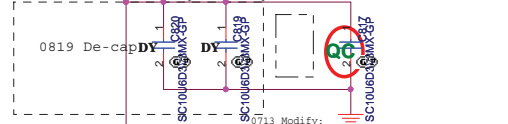
SSID = CPU

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

1115 X02 Modify:  
Reserved C802-C804, C806, C807 10uF 0603  
for power team fine tune Vcore quality.



0713 Modify:  
Removed C802, C811 10uF 0603  
cap base on layout limitation.



VCC Output Decoupling Recommendation:  
4 x 470 uF at Bottom Socket Edge  
8 x 22 uF at Top Socket Cavity  
8 x 22 uF at Top Socket Edge  
8 x 22 uF at Bottom Socket Cavity

VCC\_CORE

AG35 VCC  
AG34 VCC  
AG33 VCC  
AG32 VCC  
AG31 VCC  
AG30 VCC  
AG29 VCC  
AG28 VCC  
AG27 VCC  
AG26 VCC  
AF35 VCC  
AF34 VCC  
AF33 VCC  
AF32 VCC  
AF31 VCC  
AF30 VCC  
AF29 VCC  
AF28 VCC  
AF27 VCC  
AD35 VCC  
AD34 VCC  
AD33 VCC  
AD32 VCC  
AD31 VCC  
AD30 VCC  
AD29 VCC  
AD28 VCC  
AD27 VCC  
AC35 VCC  
AC34 VCC  
AC33 VCC  
AC32 VCC  
AC31 VCC  
AC30 VCC  
AC29 VCC  
AC28 VCC  
AC27 VCC  
AC26 VCC  
AA35 VCC  
AA34 VCC  
AA33 VCC  
AA32 VCC  
AA31 VCC  
AA30 VCC  
AA29 VCC  
AA28 VCC  
AA27 VCC  
Y35 VCC  
Y34 VCC  
Y33 VCC  
Y32 VCC  
Y31 VCC  
Y30 VCC  
Y29 VCC  
Y28 VCC  
Y27 VCC  
Y26 VCC  
Y25 VCC  
Y24 VCC  
Y23 VCC  
Y22 VCC  
Y21 VCC  
Y20 VCC  
Y19 VCC  
Y18 VCC  
Y17 VCC  
Y16 VCC  
Y15 VCC  
Y14 VCC  
Y13 VCC  
Y12 VCC  
Y11 VCC  
Y10 VCC  
Y9 VCC  
Y8 VCC  
Y7 VCC  
Y6 VCC  
Y5 VCC  
Y4 VCC  
Y3 VCC  
Y2 VCC  
Y1 VCC  
U35 VCC  
U34 VCC  
U33 VCC  
U32 VCC  
U31 VCC  
U30 VCC  
U29 VCC  
U28 VCC  
U27 VCC  
U26 VCC  
U25 VCC  
U24 VCC  
U23 VCC  
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U19 VCC  
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U17 VCC  
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U15 VCC  
U14 VCC  
U13 VCC  
U12 VCC  
U11 VCC  
U10 VCC  
U9 VCC  
U8 VCC  
U7 VCC  
U6 VCC  
U5 VCC  
U4 VCC  
U3 VCC  
U2 VCC  
U1 VCC  
R35 VCC  
R34 VCC  
R33 VCC  
R32 VCC  
R31 VCC  
R30 VCC  
R29 VCC  
R28 VCC  
R27 VCC  
R26 VCC  
R25 VCC  
R24 VCC  
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R18 VCC  
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R16 VCC  
R15 VCC  
R14 VCC  
R13 VCC  
R12 VCC  
R11 VCC  
R10 VCC  
R9 VCC  
R8 VCC  
R7 VCC  
R6 VCC  
R5 VCC  
R4 VCC  
R3 VCC  
R2 VCC  
R1 VCC

SANDY  
62.10055.421  
2nd = 62.10040.771

CORE SUPPLY

PEG AND DDR

POWER

SANDY

SENSE LINES

SVID

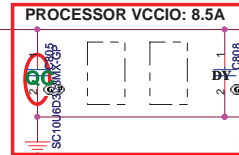
VIDALERT#  
VIDSCCLK  
VIDSOUTVCC\_SENSE  
VSS\_SENSEVCCIO\_SENSE  
VSSIO\_SENSE

GP

A00 0103 add 3rd foxconn CPU at XBuild batch run

1st = 62.10055.321

VCCIO Output Decoupling Recommendation:  
2 x 330 uF (3 x 330 uF for 2012 capable designs)  
5 x 22 uF & 5 x 0805 no-stuff at Bottom  
7 x 22 uF & 2 x 0805 no-stuff at Top



0713 Modify:  
Removed C810, C806, C807 10uF 0603  
base on layout limitation.

No-stuff sites outside the socket may be removed.  
No-stuff sites inside the socket cavity need to remain.

0617 Modify:  
Joseph Removed C812,  
C813, C814

For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7  
For CRB VIDALERT# need to pull high 75 ohm close to CPU

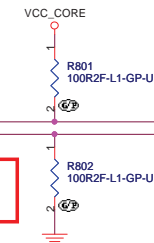


20100610 V1.0

0705 Modify:  
Removed R805, R806, already PH closed PWM side.

AJ29 H.CPU\_SVIDALRT# R803 1 43R2J-GP  
AJ30 H.CPU\_SVIDCLK  
AJ28 H.CPU\_SVIDDAT

VR\_SVID\_ALERT# 42  
H.CPU\_SVIDCLK 42  
H.CPU\_SVIDDAT 42



VCCSENSE 42  
VSSSENSE 42

VCCIO\_SENSE 45  
VSSIO\_SENSE 45

&lt;Core Design&gt;



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VCC CORE)	
Size	Document Number	Rev
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SSID = CPU

VAXG Output Decoupling Recommendation:  
2 x 470 uF at Bottom Socket Edge  
2 x 22 uF at Top Socket Cavity  
4 x 22 uF at Top Socket Edge  
2 x 22 uF at Bottom Socket Cavity  
4 x 22 uF at Bottom Socket Edge

0726 Modify:  
un-stuff C906.

VCC\_GFXCORE

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

0624 Modify:  
Removed C918,C919 10uF 0603 for VCC\_GFXCORE.

0713 Modify:  
Removed C907 10uF 0603 cap.  
0726 Modify:  
stuff C908 10uF.

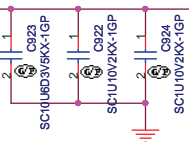
Removed DIS\_ONLY Disable Resistor.  
R904,R905,R901,R903

Disabling Guidelines for External Graphics Designs:  
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.  
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V\_S0

0617 Modify:  
Joseph Removed TC902,  
TC903 330uF cap.

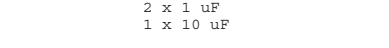
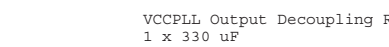
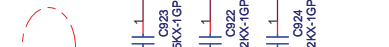
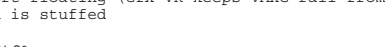
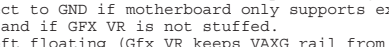
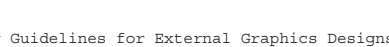
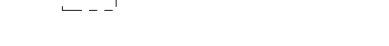
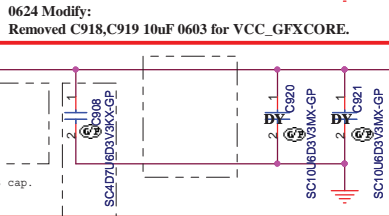
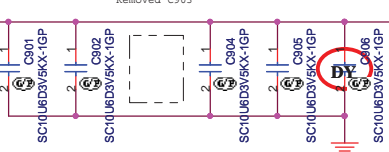
PROCESSOR VCCPLL: 1.2A



VCCPLL Output Decoupling Recommendation:  
1 x 330 uF  
2 x 1 uF  
1 x 10 uF

0721 Modify:  
Removed C903

PROCESSOR VAXG: 33A



POWER

7 OF 9

SANDY

VAXG\_SENSE  
VSSAXG\_SENSE

AK35 >>> VCC\_AXG\_SENSE 42  
AK34 >>> VSS\_AXG\_SENSE 42

Refer to the latest Huron River Mainstream PDG  
(Doc# 436735) for more details on S3 power  
reduction implementation.

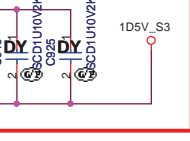
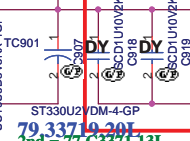
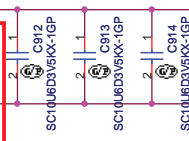
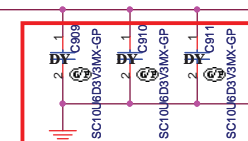
+V\_SM\_VREF\_CNT should have 10 mil trace width

SM\_VREF

AL1 <<< +V\_SM\_VREF\_CNT 37

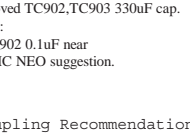
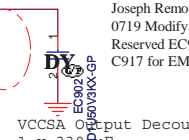
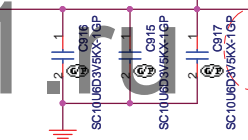
Routing Guideline:  
Power from DDR\_VREF\_S3 and +V\_SM\_VREF\_CNT  
should have 10 mils trace width.

PROCESSOR VDDQ: 10A



VDDQ Output Decoupling Recommendation:  
1 x 330 uF  
6 x 10 uF

PROCESSOR VCCSA: 6A



VCCSA Output Decoupling Recommendation:  
1 x 330 uF  
2 x 10 uF at Bottom Socket Cavity  
1 x 10 uF at Bottom Socket Edge

0624 Modify:  
Removed R902 10ohm closed CPU side.

0713 Modify:  
Add R908 100ohm PH to 0D85V\_S0.

0714 Modify:  
Removed R908 PH.

0714 Modify:  
Removed R908 PH.

0714 Modify:  
Removed R908 PH.

0714 Modify:  
Removed R908 PH.

0714 Modify:  
Removed R908 PH.

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Removed R908 PH.

DCBATOUT



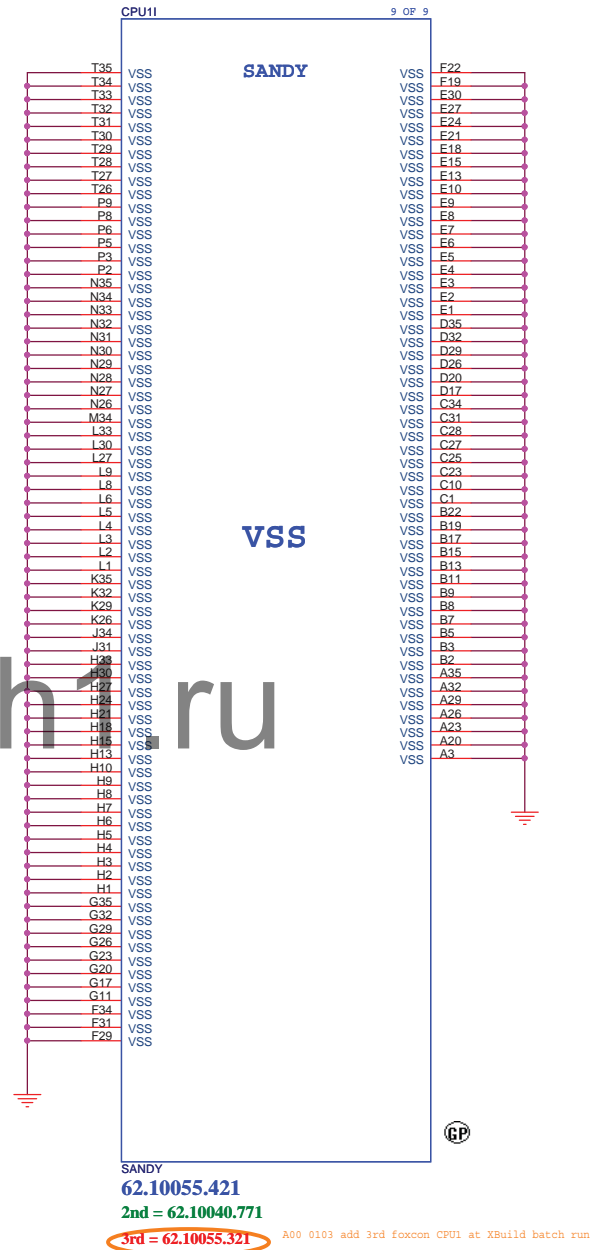
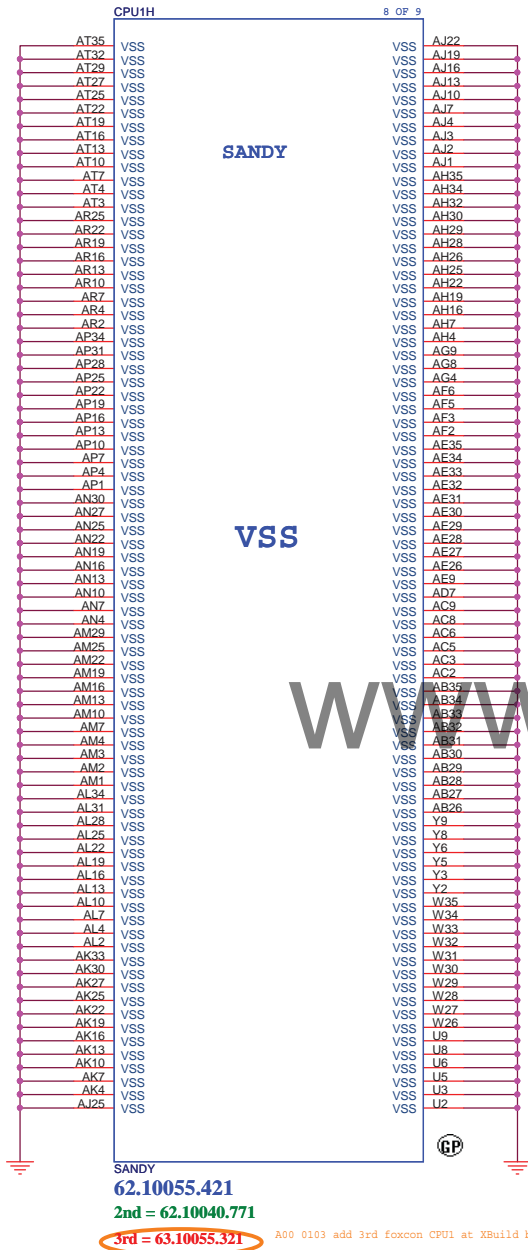
1122 X02 Modify:  
stuff EC901 0.1uF from  
EMC Neo suggestion.

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title	CPU (VCC GFXCORE)		
Size	Document Number	Rev	A00
A3		QUEEN 15	
Date:	Tuesday, January 04, 2011	Sheet	9 of 108

SSID = CPU






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<Variant Name>			
		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>XDP</b>			
Size A3	Document Number <b>QUEEN 15</b>		Rev <b>A00</b>
Date: Tuesday, January 04, 2011	Sheet 11	of 108	

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Title

*Reserved*


Size	Document Number	Rev
A3	<b>QUEEN 15</b>	<b>A00</b>

Date: Tuesday, January 04, 2011	Sheet 12 of 108
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Title

*Reserved*

Size	Document Number	Rev
A3	<b>QUEEN 15</b>	<b>A00</b>

Date: Tuesday, January 04, 2011	Sheet 13 of 108
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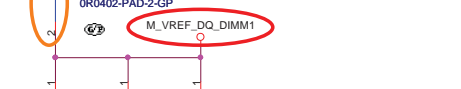
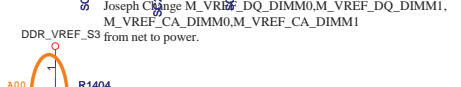
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0624 Modify:  
SWAP DM1 and DM2 location.

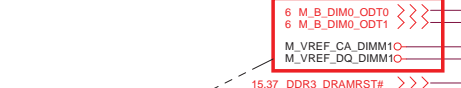
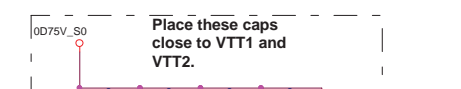
0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



0707 Modify:  
Change R1404, R1405 to 0ohm 0402 from short pad.



0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0, M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0, M\_VREF\_CA\_DIMM1  
from net to power.



- M\_B A0 98
- M\_B A1 97
- M\_B A2 96
- M\_B A3 95
- M\_B A4 94
- M\_B A5 93
- M\_B A6 92
- M\_B A7 91
- M\_B A8 90
- M\_B A9 89
- M\_B A10 88
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- M\_B A94 4
- M\_B A95 3
- M\_B A96 2
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- M\_B A98 0

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- M\_B BS0 >>>
- M\_B BS1 >>>
- M\_B DQ[63:0] >>>

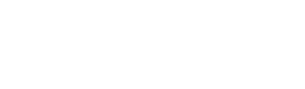
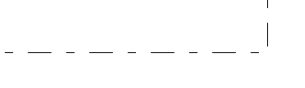
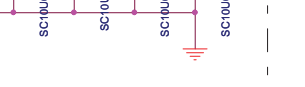
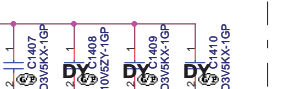
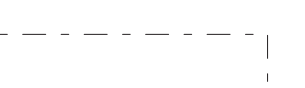
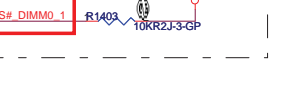
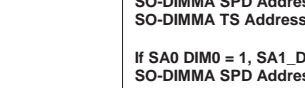
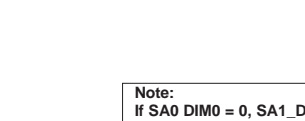
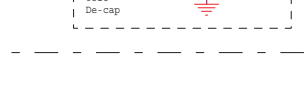
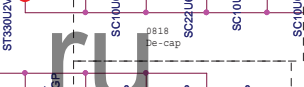
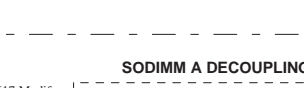
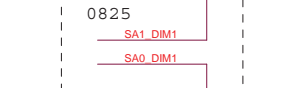
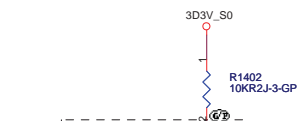
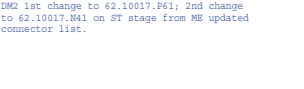
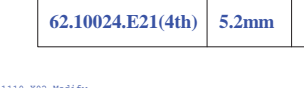
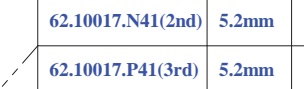
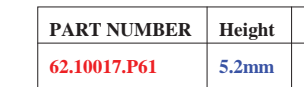
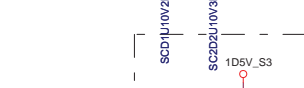
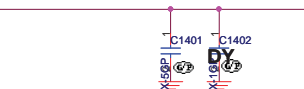
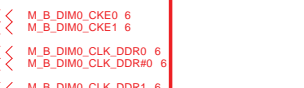
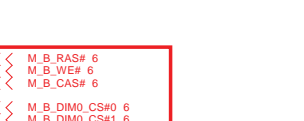
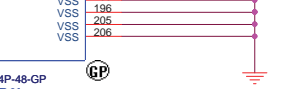
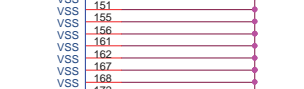
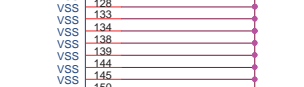
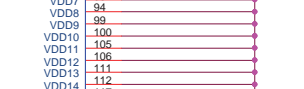
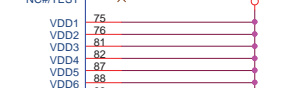
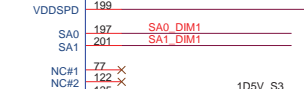
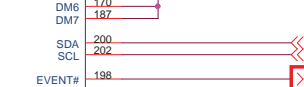
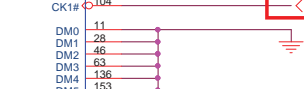
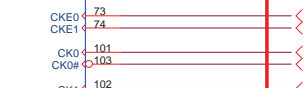
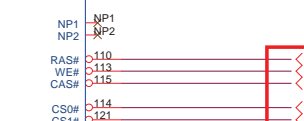
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- M\_B DQS#5 154
- M\_B DQS#6 171
- M\_B DQS#7 188

- 6 M\_B\_DIM0\_ODT0 >>>
- 6 M\_B\_DIM0\_ODT1 >>>
- M\_VREF\_CA\_DIMM1 >>>
- M\_VREF\_DQ\_DIMM1 >>>

- 15,37 DDR3\_DRAMRST# >>>
- 0D75V\_S0 >>>
- VTT1 >>>
- VTT2 >>>

- H = 5.2mm
- DDR3-204P-48-GP
- 62.10017.P61
- 2nd = 62.10017.N41
- 3rd = 62.10017.P41
- 4th = 62.10024.E21

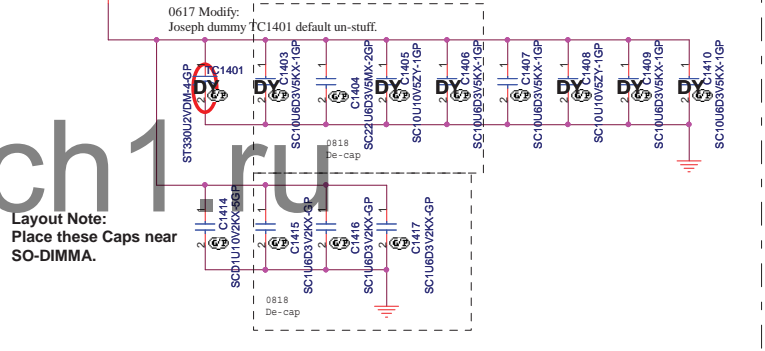


Note:  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

## Thermal EVENT



## SODIMM A DECOUPLING



Layout Note:  
Place these Caps near  
SO-DIMMA.

PART NUMBER	Height	TYPE
62.10017.P61	5.2mm	REVERSED
62.10017.N41(2nd)	5.2mm	REVERSED
62.10017.P41(3rd)	5.2mm	REVERSED
62.10024.E21(4th)	5.2mm	REVERSED

1110 X02 Modify:  
DM2 1st change to 62.10017.P61; 2nd change  
to 62.10017.N41 on ST stage from ME updated  
connector list.

<Variant Name>

**Wistron Corporation**  
21F, 88, Sec.1, Han Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM2**

Size: **QUEEN 15**

Date: **1/04/2011**

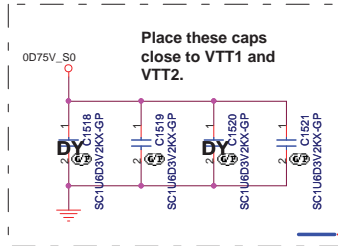
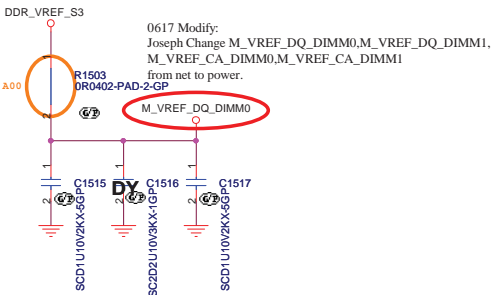
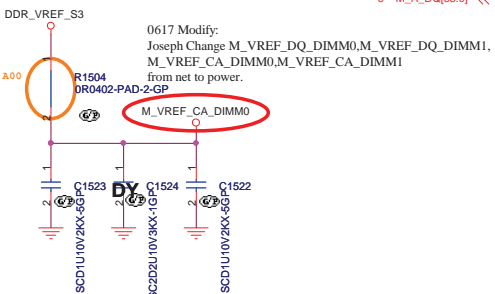
Document Number: **A00**

Rev: **14**

Sheet: **14** of **108**

**SSID = MEMORY**

0707 Modify:  
Change R1503,R1504 to 0ohm 0402 from short pad.

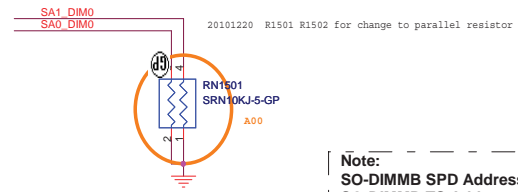
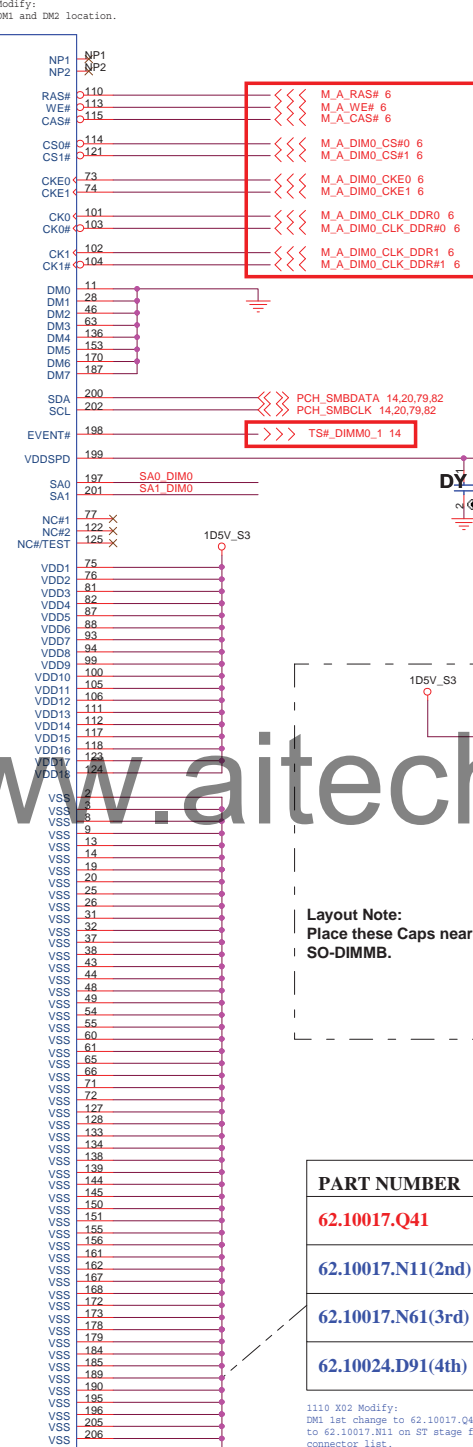


0617 Modify:  
Joseph Change M\_VREF\_DQ\_DIMM0,M\_VREF\_DQ\_DIMM1,  
M\_VREF\_CA\_DIMM0,M\_VREF\_CA\_DIMM1  
from net to power.

H = 9.2mm

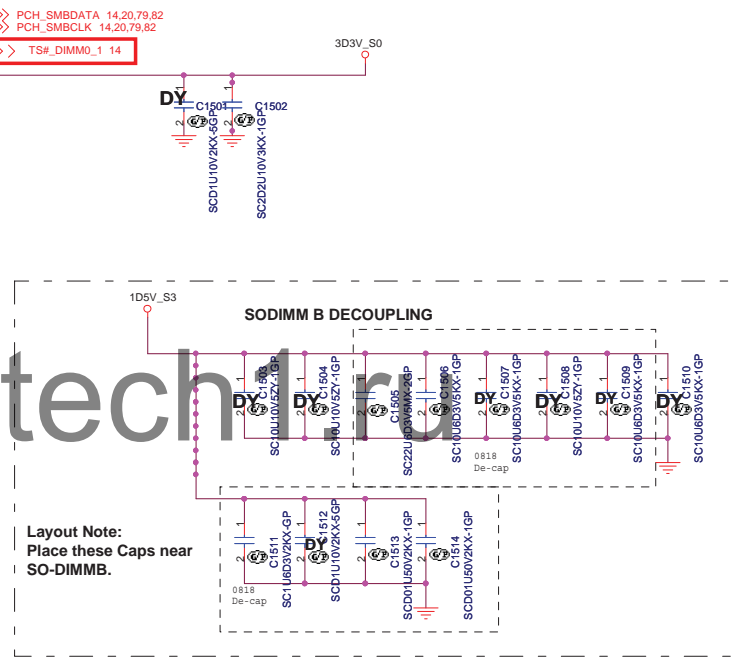
DDR3-204P-42-GP

62.10017.Q41  
2nd = 62.10017.N11  
3rd = 62.10017.N61  
4th = 62.10024.D91



Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



**Layout Note:**  
Place these Caps near  
SO-DIMMB.

PART NUMBER	Height	TYPE
62.10017.Q41	9.2mm	REVERSED
62.10017.N11(2nd)	9.2mm	REVERSED
62.10017.N61(3rd)	9.2mm	REVERSED
62.10024.D91(4th)	9.2mm	REVERSED

1110 X02 Modify:  
DM1 1st change to 62.10017.Q41; 2nd change  
to 62.10017.N11 on ST stage from ME updated  
connector list.

<Variant Name>




**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>DDR3-SODIMM1</b>			
Size Custom	Document Number		Rev
	<b>QUEEN 15</b>		<b>A00</b>
Date:	Tuesday, January 04, 2011	Sheet 15 of	108

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<Core Design>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

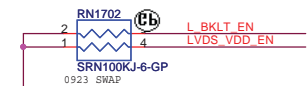
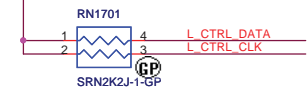
**Reserved**

Size	Document Number	Rev
A3	<b>QUEEN 15</b>	<b>A00</b>

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---------------------------------	-----------------



3D3V\_S0



**L\_DDC\_DATA(PAGE17):**  
This signal is on the LVDS interface.  
This signal needs to be left NC if eDP is  
used for the local flat panel display

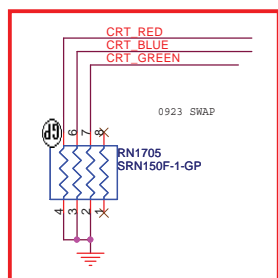
Place near PCH

Impedance: 90 ohm

0617 Modify:  
Joseph Removed LVDSB related net for  
single LVDS channel base on Dell updated spec.

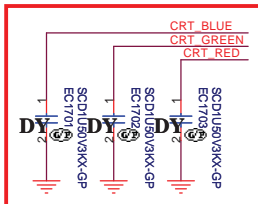
0917 X01 Modify:  
Add R1703-R1705 on RGB signal and reserved  
EC1701-EC1703 0.1u from EMC Neo suggestion.

Close to PCH side



82 CRT\_BLUE  
82 CRT\_GREEN  
82 CRT\_RED

Notes:  
1K 0.5% 0402.  
CHIP RES 1K D 1/16W 0402



Notes:  
1K 0.5% 0402.  
CHIP RES 1K D 1/16W 0402

PCH1D

Cougar  
Point

4 OF 10

Digital Display Interface

LVDS

CRT

COUGAR-GP-U2-NF

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-A	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
PORT-B	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIIB_CTRLDATA

&lt;Variant Name&gt;



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Title

**PCH (LVDS/CRT/DDI)**

Size

Document Number

**QUEEN 15**

Rev

**A00**

Date: Tuesday, January 04, 2011

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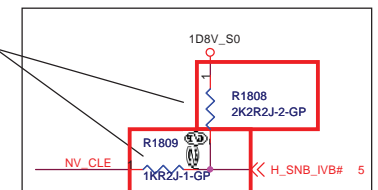
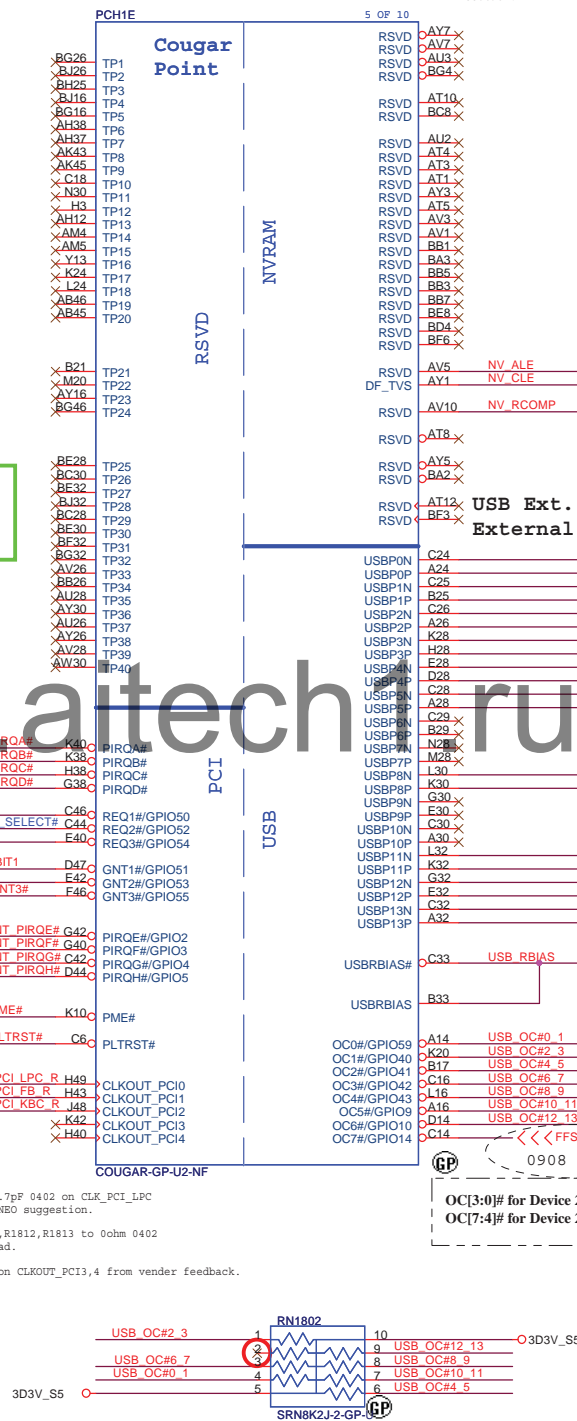
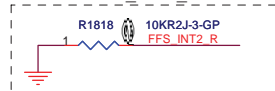
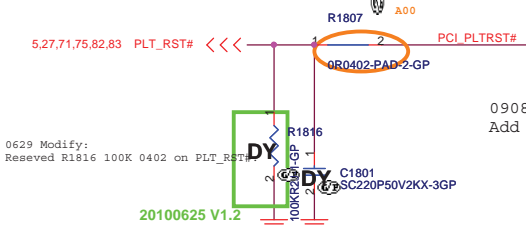
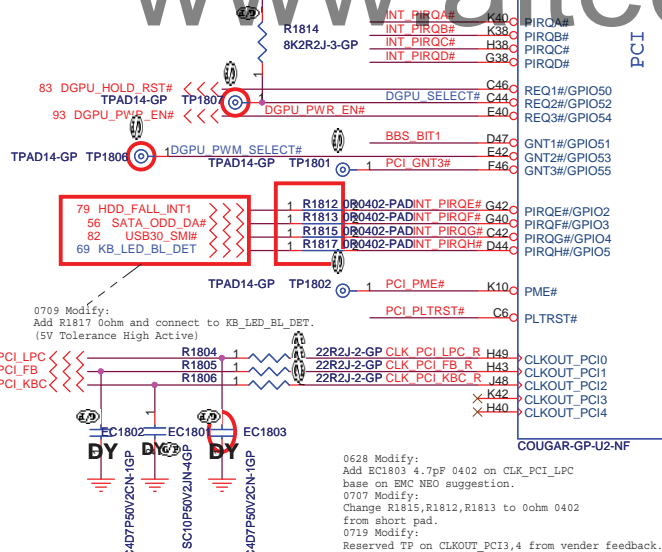
```
0709 Modify:
Removed INT_PIRQH# on RN1801 pin1.
```



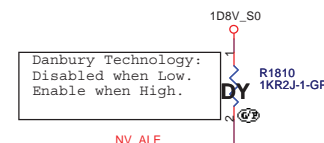
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



External debug port use on Huron river platform

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB C
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Card

```
1120 X02 Modify:
Reserved USB OC#0 1 connect from PCH GPIO59.
```

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used



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Title			
<b>PCH (PCI/USB/NVRAM)</b>			
Size A3	Document Number		Rev
	<b>QUEEN 15</b>		<b>A0</b>
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**SSID = PCH**

4 DMI\_RXN[3:0]      

4 DMI\_RXP[3:0]      

4 DMI\_TXN[3:0]      

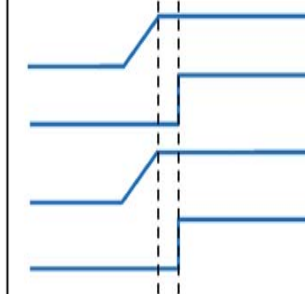
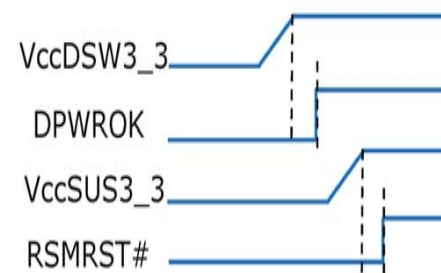
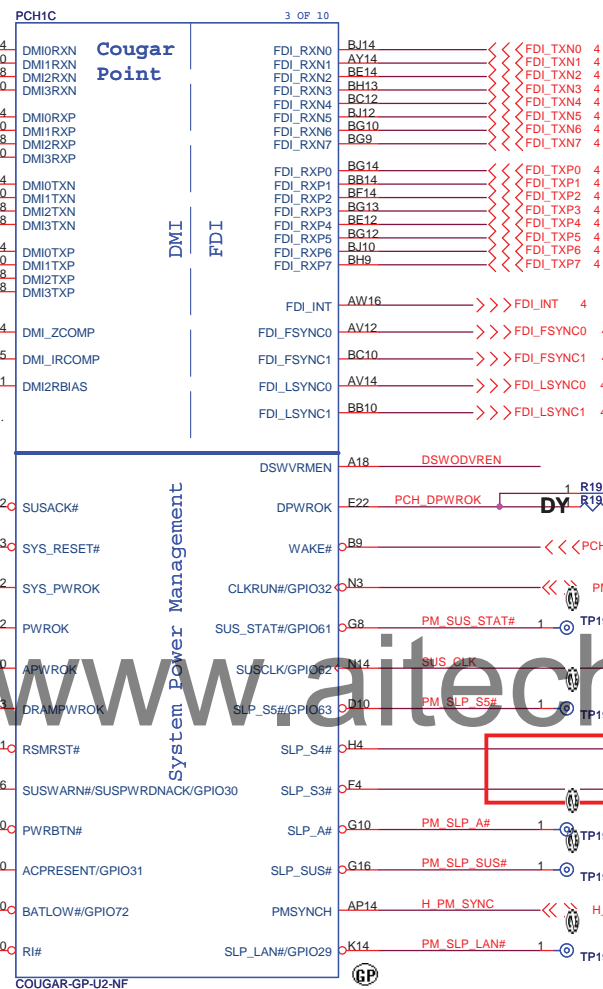
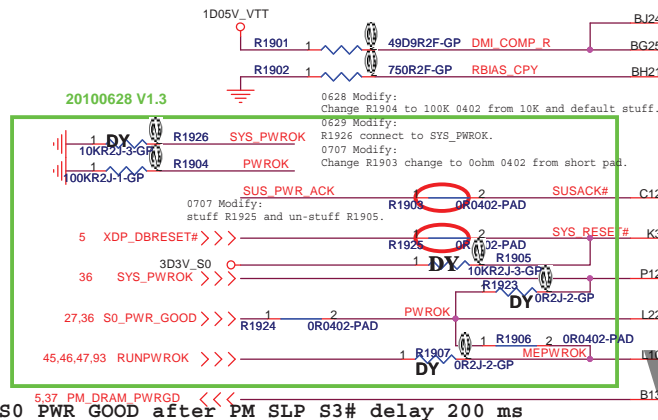
4 DMI\_TXP[3:0]      

	FDI_TXN[7:0]	4
	FDI_TXP[7:0]	4

## Deep S4/S5 Supported

Deep S4/S5 **Not** Supported

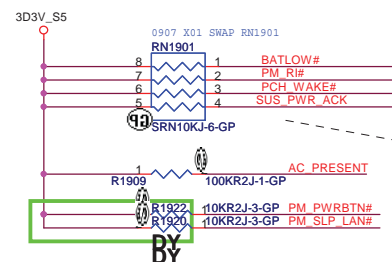
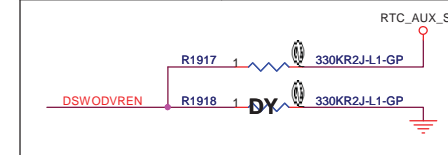
Signal Routing Guideline:  
DMI\_ZCOMP keep W=4 mils and  
routing length less than 500  
mils.  
DMI\_IRCOMP keep W=4 mils and  
routing length less than 500  
mils.



**For platforms not supporting Deep S4/S5**

- 1.VccSUS3\_3 and VccDSW3\_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP\_SUS# and SUSACK# are left as {Y}no connect;
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

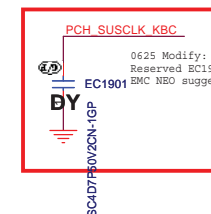


```
PCIE_WAKE#
CRB : 1K
_CEKLT: 10K
```

```
0920 X01 Modify:
      move PCH_WAKES# to RN1901 pin4
      Add R1909 PH on AC_PRESENT.
```

0719 Modify:  
 Change R1908 to 10K ohm based on Intel review:  
 8.2K to 10K pull-down is recommended.

0621 Modify:  
Joseph removed Q1901/R1909/R1916 3V\_5V\_POK  
and PM\_RSMRST# related control circuit.



<Variant Name>



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Title		<b>PCH (DM I/FDI/PM)</b>	
Size A3	Document Number	<b>QUEEN 15</b>	Rev <b>A0</b>
Date:	Tuesday, January 04, 2011	Sheet 19 of	108

SSID = PCH

1112 X02 Modify:  
Dell required us to disable PCIE port of WWAN slot  
If PCIE port 1 is disabled, it will cause all PCIE port  
disabled, so change WWAN to PCIE port 3 from port 1  
at ST stage.

82 PCIE\_RXN2  
82 PCIE\_RXP2  
82 PCIE\_TXN2  
82 PCIE\_TXP2

82 PCIE\_RXN3  
82 PCIE\_RXP3  
82 PCIE\_TXN3  
82 PCIE\_TXP3

82 PCIE\_RXN4  
82 PCIE\_RXP4  
82 PCIE\_TXN4  
82 PCIE\_TXP4

82 PCIE\_RXN5  
82 PCIE\_RXP5  
82 PCIE\_TXN5  
82 PCIE\_TXP5

82 PCIE\_RXN6  
82 PCIE\_RXP6  
82 PCIE\_TXN6  
82 PCIE\_TXP6

82 PCIE\_RXN7  
82 PCIE\_RXP7  
82 PCIE\_TXN7  
82 PCIE\_TXP7

82 PCIE\_RXN8  
82 PCIE\_RXP8  
82 PCIE\_TXN8  
82 PCIE\_TXP8

82 CLK\_PCIE\_WWAN#  
82 CLK\_PCIE\_WWAN#

82 CLK\_PCIE\_WLAN#  
82 CLK\_PCIE\_WLAN#

82 CLK\_PCIE\_LAN#  
82 CLK\_PCIE\_LAN#

82 CLK\_PCIE\_USB3#  
82 CLK\_PCIE\_USB3#

82 CLK\_PCIE\_NEW#  
82 CLK\_PCIE\_NEW#

82 CLK\_PCIE\_NEW#  
82 CLK\_PCIE\_NEW#

82 CLK\_PCIE\_NEW#  
82 CLK\_PCIE\_NEW#

82 CLK\_PCIE\_NEW#  
82 CLK\_PCIE\_NEW#

82 CLK\_PCIE\_NEW#  
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82 CLK\_PCIE\_NEW#

82 CLK\_PCIE\_NEW#  
82 CLK\_PCIE\_NEW#

82 CLK\_PCIE\_NEW#  
82 CLK\_PCIE\_NEW#

Cougar  
Point  
Card Reader

LAN

W-WAN

WLAN

USB3.0

Intel GBE LAN

Dock

NEW CARD

SMBUS

Controller

Link

CLOCKS

FLEX CLOCKS

SMBALERT#/GPIO11  
SMBCLK  
SMBDATA

SML0ALERT#/GPIO60  
SML0CLK  
SML0DATA

SML1ALERT#/PCHHOT#/GPIO74  
SML1CLK/GPIO58  
SML1DATA/GPIO75

CL\_CLK1  
CL\_DATA1  
CL\_RST1#

CLKOUT\_PCIE0N  
CLKOUT\_PCIE0P

CLKOUT\_PCIE1N  
CLKOUT\_PCIE1P

CLKOUT\_PCIE2N  
CLKOUT\_PCIE2P

CLKOUT\_PCIE3N  
CLKOUT\_PCIE3P

CLKOUT\_PCIE4N  
CLKOUT\_PCIE4P

CLKOUT\_PCIE5N  
CLKOUT\_PCIE5P

CLKOUT\_PCIE6N  
CLKOUT\_PCIE6P

CLKOUT\_PCIE7N  
CLKOUT\_PCIE7P

CLKOUT\_PCIE8N  
CLKOUT\_PCIE8P

CLKOUT\_PCIE9N  
CLKOUT\_PCIE9P

CLKOUT\_PCIE10N  
CLKOUT\_PCIE10P

CLKOUT\_PCIE11N  
CLKOUT\_PCIE11P

CLKOUT\_PCIE12N  
CLKOUT\_PCIE12P

EC\_SW#  
SMB\_CLK  
SMB\_DATA

DRAMRST\_CNTRL\_PCH  
SML0\_CLK  
SML0\_DATA

PCH\_GPIO74  
SML1\_CLK  
SML1\_DATA

CL\_CLK  
CL\_DATA  
CL\_RST

CLK\_PCIE\_VGA#  
CLK\_PCIE\_VGA#

CLK\_EXP\_N  
CLK\_EXP\_P

CLK\_BUF\_EXP\_N  
CLK\_BUF\_EXP\_P

CLK\_BUF\_CPYCLK\_N  
CLK\_BUF\_CPYCLK\_P

CLK\_BUF\_DOT96\_N  
CLK\_BUF\_DOT96\_P

CLK\_BUF\_CKSSCD\_N  
CLK\_BUF\_CKSSCD\_P

CLK\_BUF\_REF14  
CLK\_BUF\_REF14

CLK\_PCIE\_FB  
CLK\_PCIE\_FB

CLK\_PCIE\_FB  
CLK\_PCIE\_FB

CLK\_PCIE\_FB  
CLK\_PCIE\_FB

CLK\_PCIE\_FB  
CLK\_PCIE\_FB

CLK\_PCIE\_FB  
CLK\_PCIE\_FB

CLK\_PCIE\_FB  
CLK\_PCIE\_FB

3D3V\_S5  
SMB\_CLK  
SMB\_DATA

3D3V\_S0  
SML0\_CLK  
SML0\_DATA

3D3V\_S5  
SML1\_CLK  
SML1\_DATA

3D3V\_S0  
CL\_CLK  
CL\_DATA

3D3V\_S5  
CLK\_PCIE\_VGA#  
CLK\_PCIE\_VGA#

3D3V\_S0  
CLK\_EXP\_N  
CLK\_EXP\_P

3D3V\_S5  
CLK\_BUF\_EXP\_N  
CLK\_BUF\_EXP\_P

3D3V\_S0  
CLK\_BUF\_CPYCLK\_N  
CLK\_BUF\_CPYCLK\_P

3D3V\_S5  
CLK\_BUF\_DOT96\_N  
CLK\_BUF\_DOT96\_P

3D3V\_S0  
CLK\_BUF\_CKSSCD\_N  
CLK\_BUF\_CKSSCD\_P

3D3V\_S5  
CLK\_BUF\_REF14  
CLK\_BUF\_REF14

3D3V\_S0  
CLK\_PCIE\_FB  
CLK\_PCIE\_FB

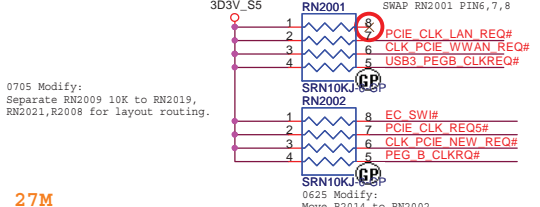
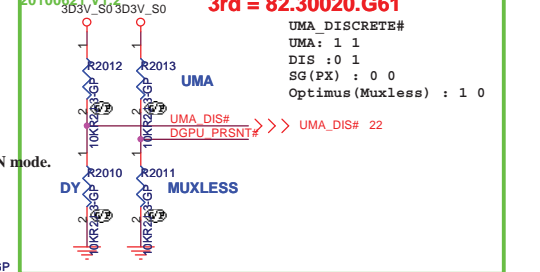
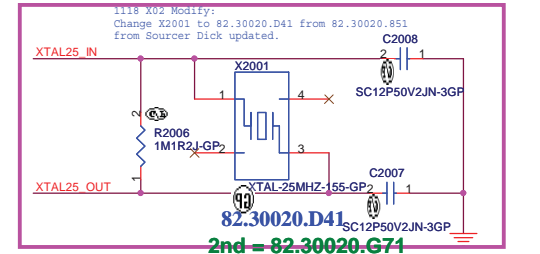
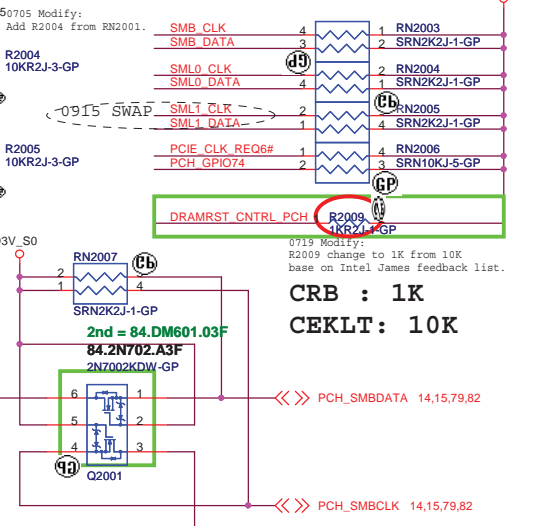
3D3V\_S5  
CLK\_PCIE\_FB  
CLK\_PCIE\_FB

3D3V\_S0  
CLK\_PCIE\_FB  
CLK\_PCIE\_FB

3D3V\_S5  
CLK\_PCIE\_FB  
CLK\_PCIE\_FB

3D3V\_S0  
CLK\_PCIE\_FB  
CLK\_PCIE\_FB

3D3V\_S5  
CLK\_PCIE\_FB  
CLK\_PCIE\_FB



**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

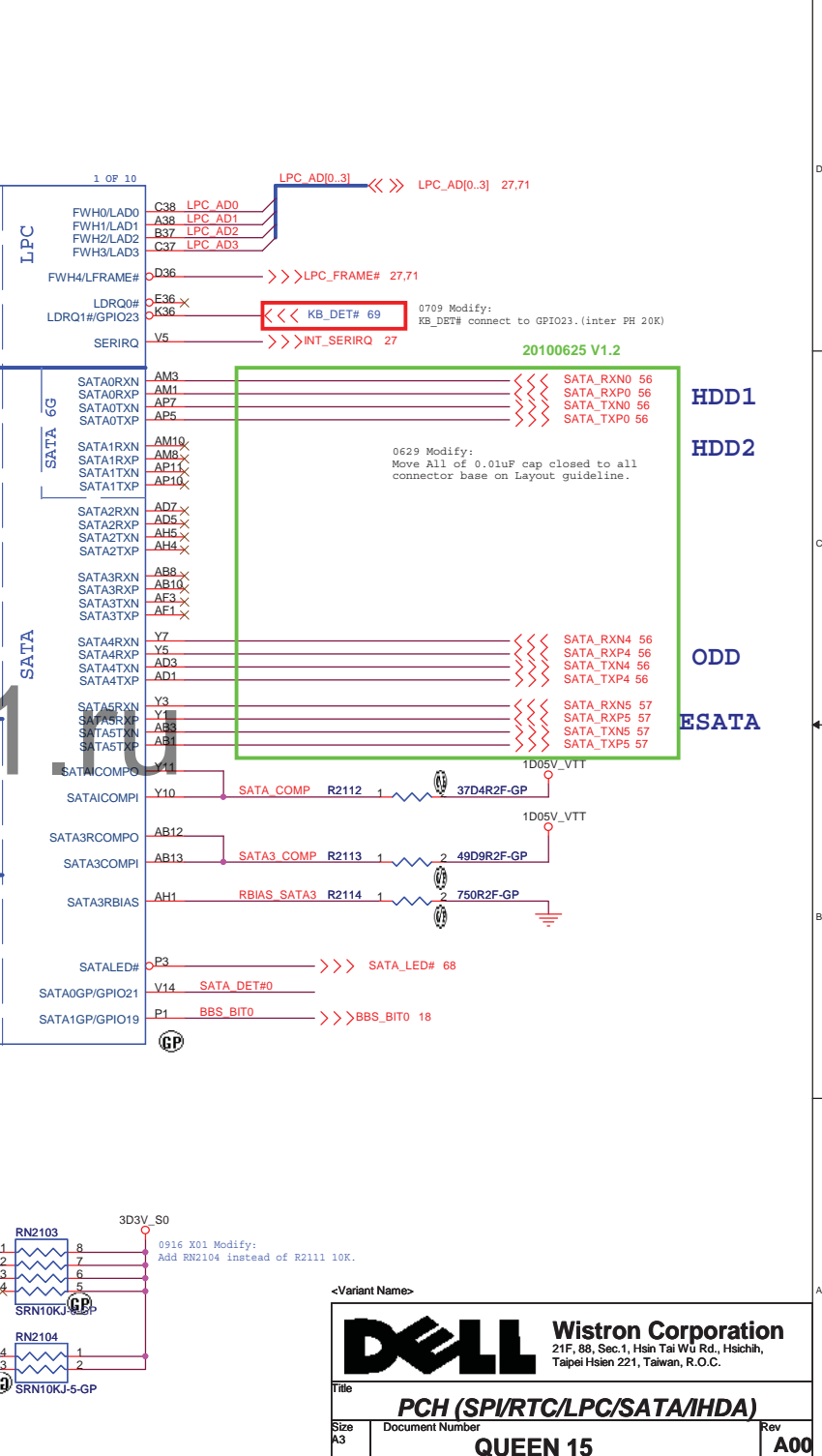
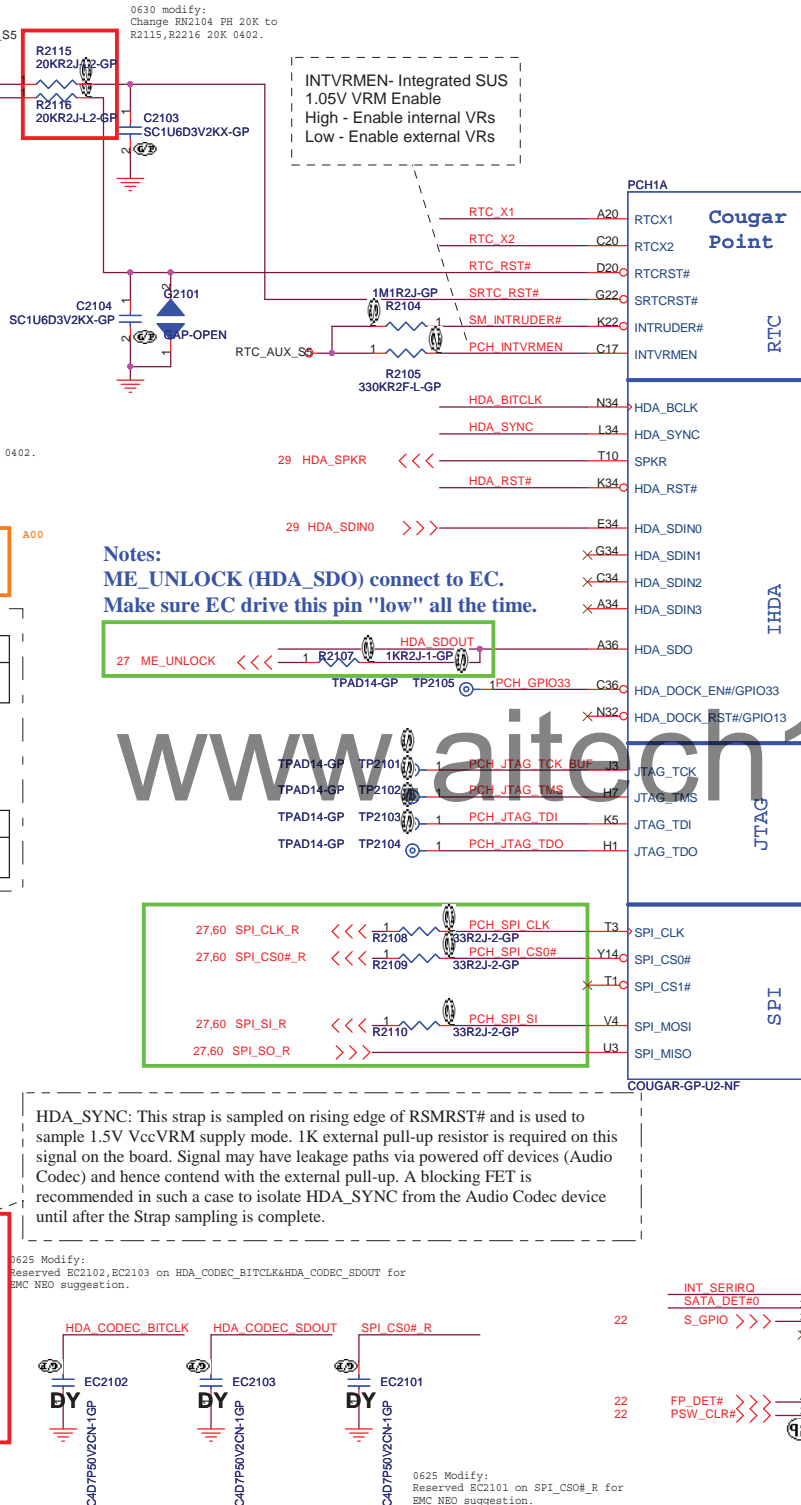
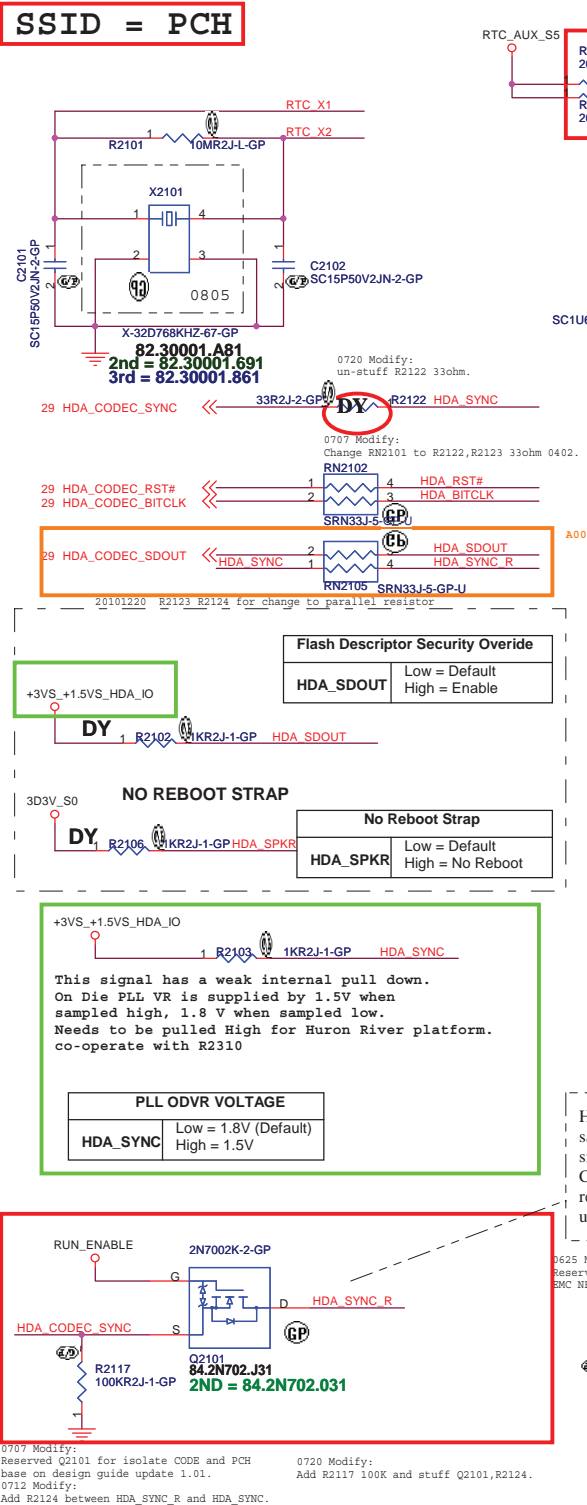
Size: A3 Document Number: **QUEEN 15** Rev: **A00**

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1V Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3  
1V Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2  
if more than 2 PCI clocks + PCI loopback are routed.



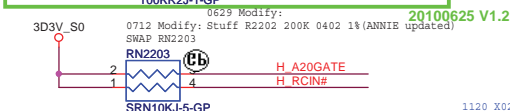
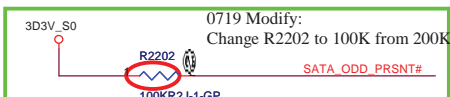
SSID = PCH



# SSID = PCH

Note:  
For PCH debug with XDP, need to NO STUFF R2218

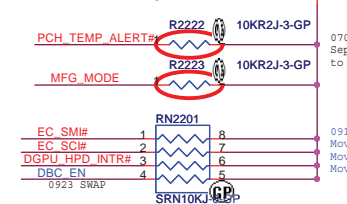
	GSENSOR_ST	GSENSOR_ADI
R2205	DY	10K
R2206	100K	DY



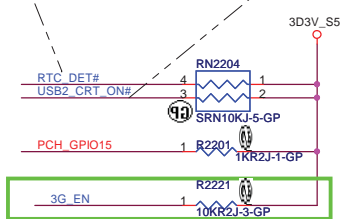
GPIO27 has a weak[20K] internal pull up.  
To enable on-die PLL Voltage regulator,  
should not place external pull down.



0701 Modify:  
Separate PCH\_TEMP\_ALERT# from RN2201  
to R2222 10K base on layout limitation.



1120 X02 Modify:  
Rename PCH\_GPIO12 to RTC\_DET#  
on GPIO12.



20100625 V1.2

0629 Modify:  
Add R2221 10K 0402 on PCH\_GPIO124 (ANNIE updated)  
0709 Modify:  
Rename PCH\_GPIO124 to 3G\_EN on R2221.

1120 X02 Modify:  
Rename PCH\_GPIO12 to RTC\_DET#  
on GPIO12.

0908 X01 Modify:  
change FFS INT2\_R from PCH\_GPIO148 to GPIO14  
keep PCH\_GPIO15 PH R2201, PCH\_GPIO148 PH R2220

0720 Modify:  
Removed DBC\_EN on GPIO22.

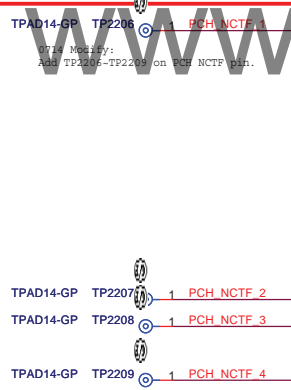
0709 Modify:  
Rename PCH\_GPIO122 to DBC\_EN.  
Rename PCH\_GPIO124 to 3G\_EN.

0701 Modify:  
Separate MFG\_MODE from RN2202  
to R2223 10K base on layout limitation.

0916 X01 Modify:  
Move EC\_SCIN#, DBC\_EN to RN2201.  
Move S\_GPIO to RN2103.  
Move PSW\_CLR# to RN2104.

1118 X02 Modify:  
Rename GFX\_CRB\_DET to GSENSOR\_DET  
on GPIO39.

1120 X02 Modify:  
Reserved USB2\_CRT\_ON# to control  
U6102 USB power switch from PCH\_GPIO157.



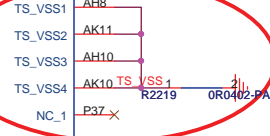
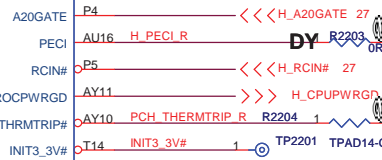
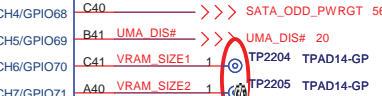
[VRAM\_SIZE1:VRAM\_SIZE2]  
LL=512M / HL=1G / LH=2G

0705 Modify:  
Removed R2214-R2217 10K 0402 on VRAM\_SIZE1&2.

Cougar Point

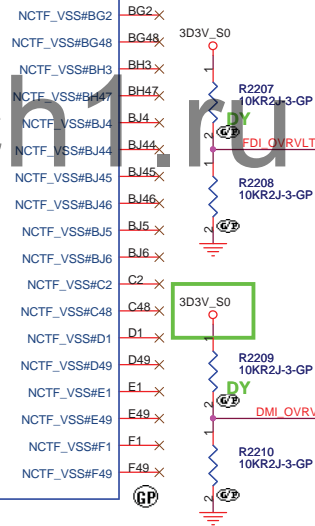


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TS Signal Disable Guideline:  
TS\_VSS1, TS\_VSS2, TS\_VSS3 and TS\_VSS4  
should not float on the motherboard. They should  
be tied to GND directly.

0707 Modify:  
Change R2219 change to 0ohm 0402 from short pad.



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPI08 has a weak[20K] internal pull up.  
Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

PLL ON DIE VR ENABLE	
NOTE: This signal has a weak internal pull-up 20K	
ENABLED -- HIGH (R2212 UNSTUFFED)	DEFAULT
DISABLED -- LOW (R2212 STUFFED)	



<Variant Name>

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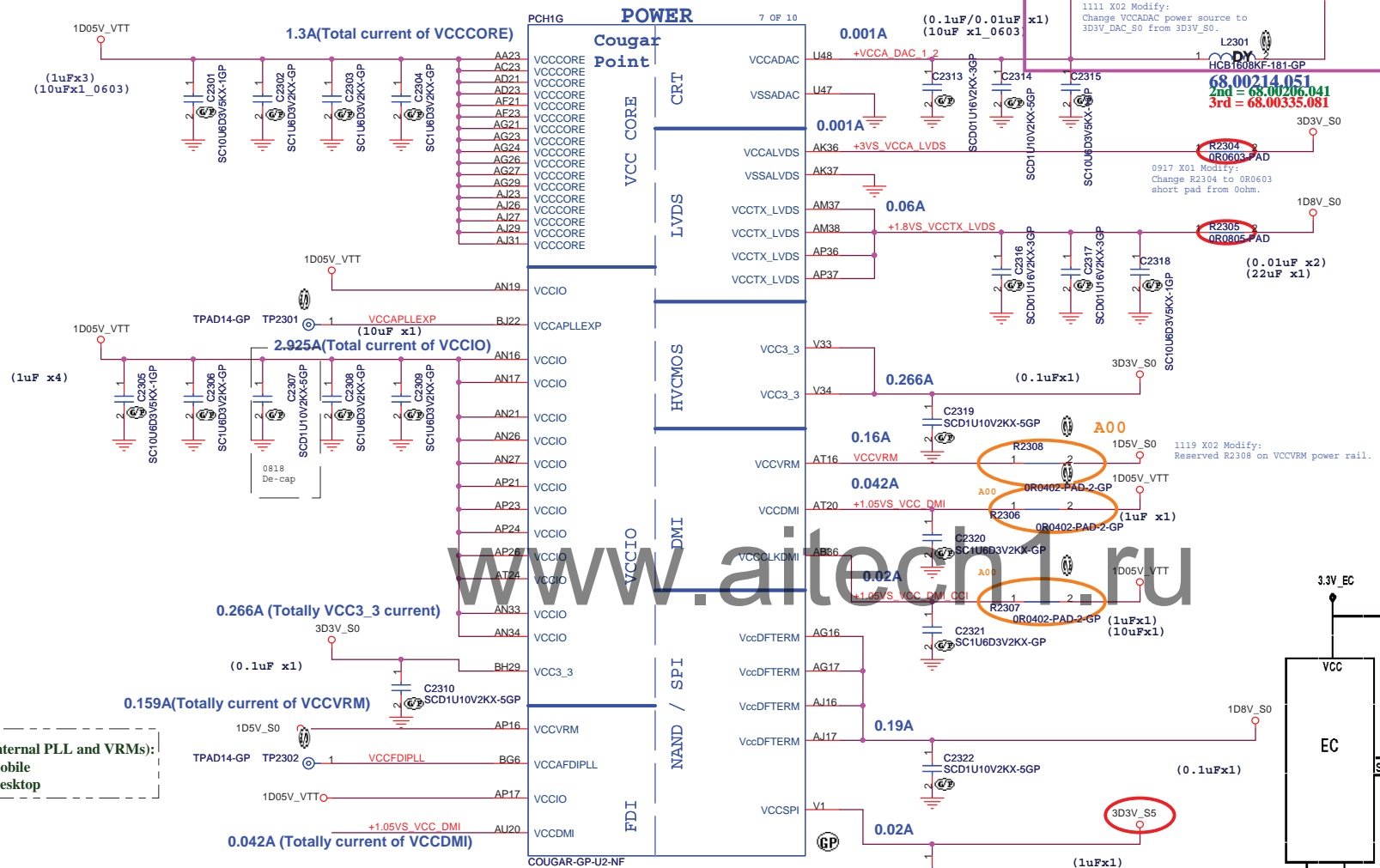
Title: **PCH (GPIO/CPU)**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

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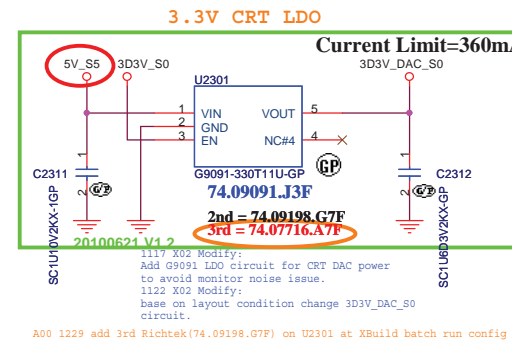
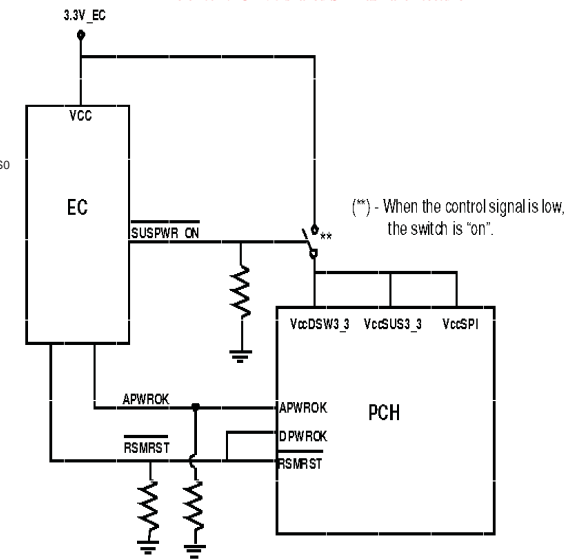


**SSID = PCH 6A**



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

**Refer to NPCE795 shared SPI flash architecture**



<Variant Name>



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Title

**PCH (POWER1)**

Size

Document Number

**QUEEN 15**

Rev

Date: Tuesday, January 04, 2011

Sheet

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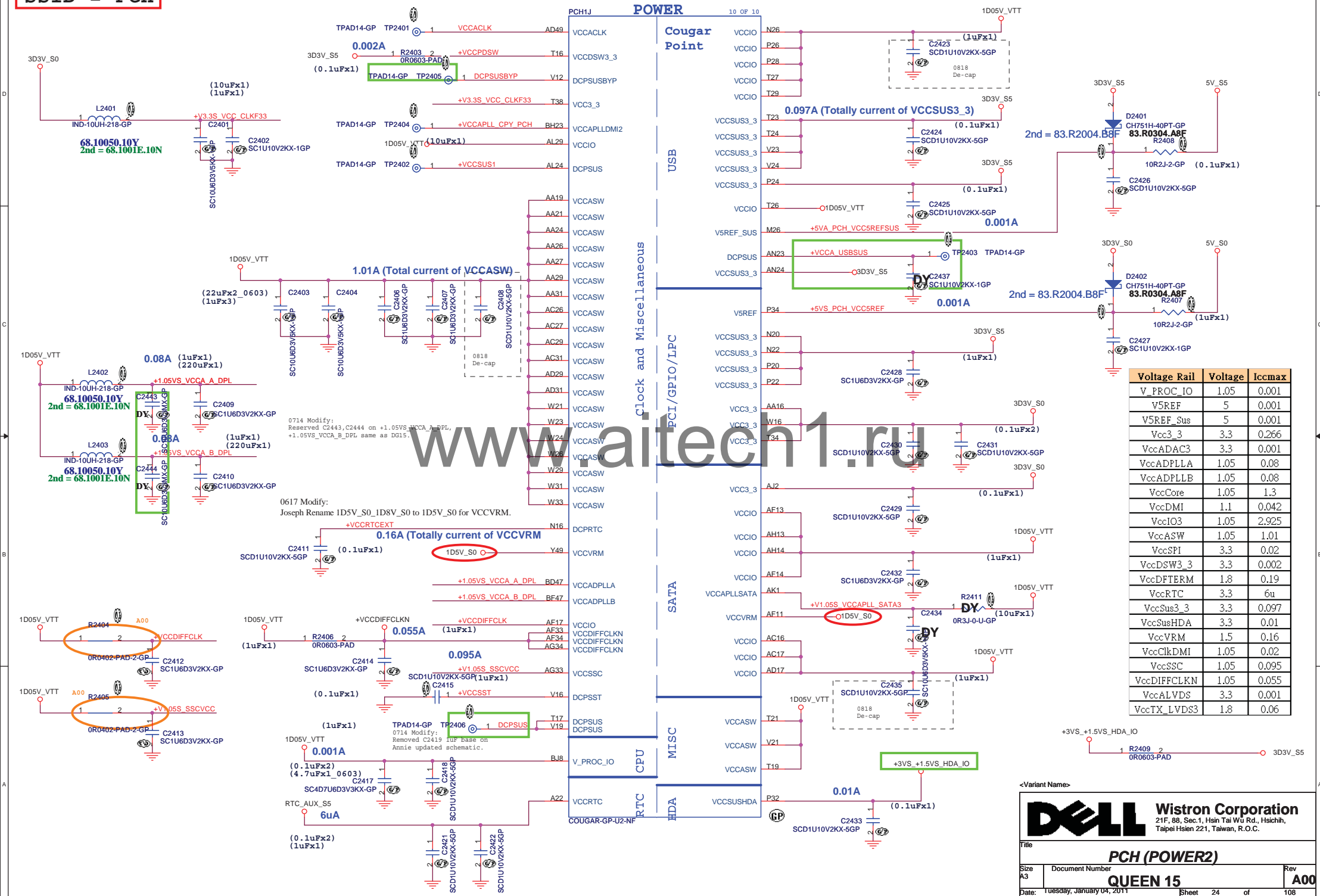
23

of

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108

SSID = PCH



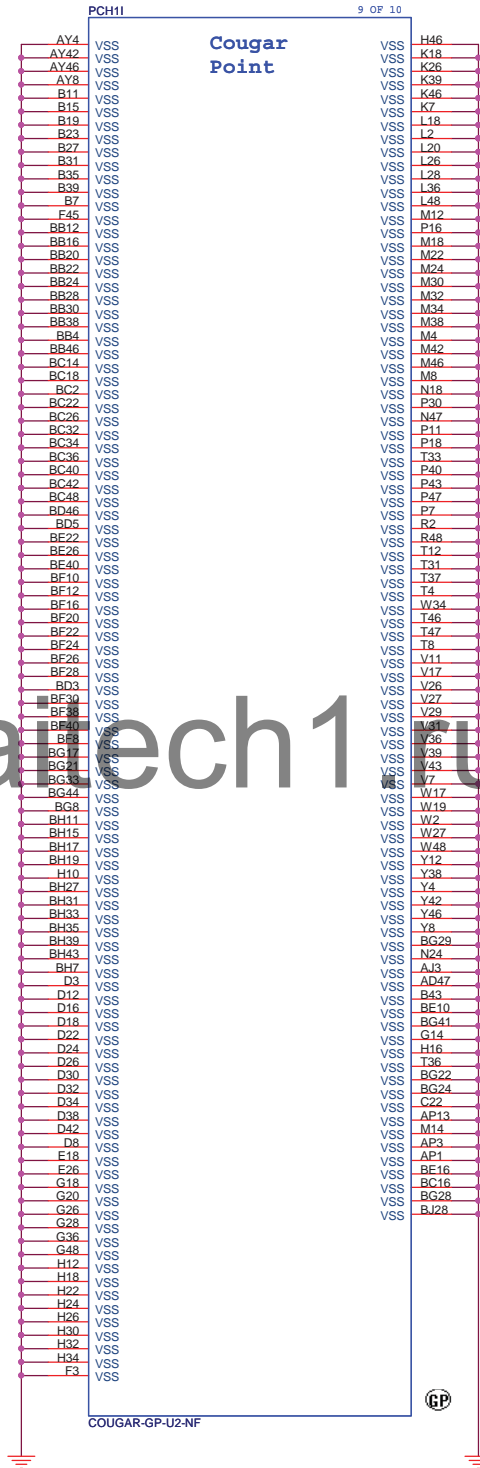
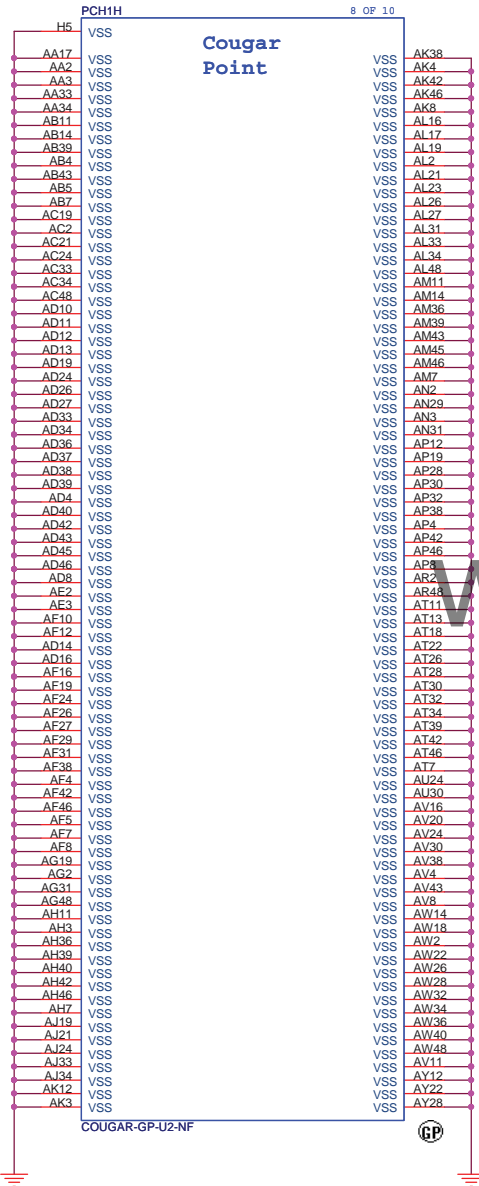
Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLL	1.05	0.08
VccADPLL	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTerm	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

&lt;Variant Name

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Title			
<b>PCH (POWER2)</b>			
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SSID = PCH



<Variant Name>

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**PCH (VSS)**

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<Variant Name>



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Title

*Reserved*

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5

3

3



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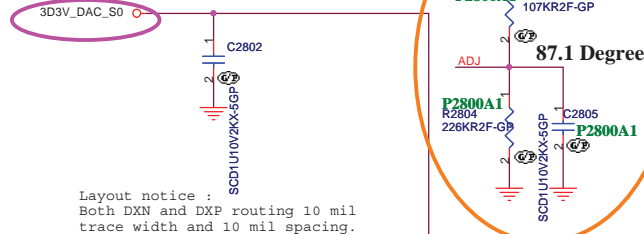
SSID = Thermal

## Thermal sensor P2800

0705 Modify:  
R2802 change to 0ohm 0402 from short pad and default un-stuff.

## Fan controller P2793

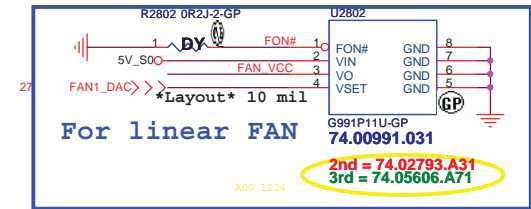
1119 X02 Modify:  
Change U2801,U2804,U2805 VCC power to 3D3V\_DAC\_S0 from 3D3V\_S0.



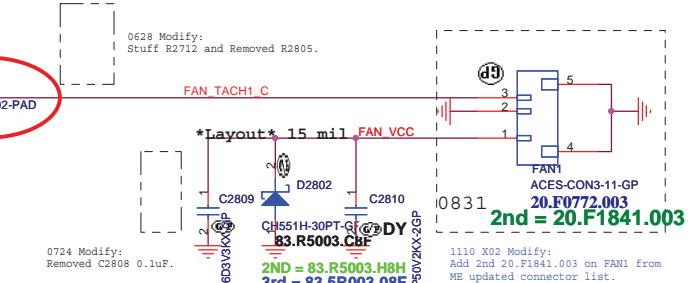
A00 1227

1111 X02 Modify:  
ADJ&ADJ\_VGA power source change to 3D3V\_DAC\_S0 from 3D3V\_S0 to solve T8 shut down issue.

1227 A00 Modify:  
If stuff P2800E21 then must stuff R2803,R2804,C2805 but if stuff P2800E30 should be unstuff.



0614 Modify:  
Change FAN1 connector part number to 20.D0210.103 base on ME EMN and DXF.  
0712 Modify:  
Change FAN1 part number to 20.F1639.004 from 20.D0210.103 base on latest EMN and DXF.



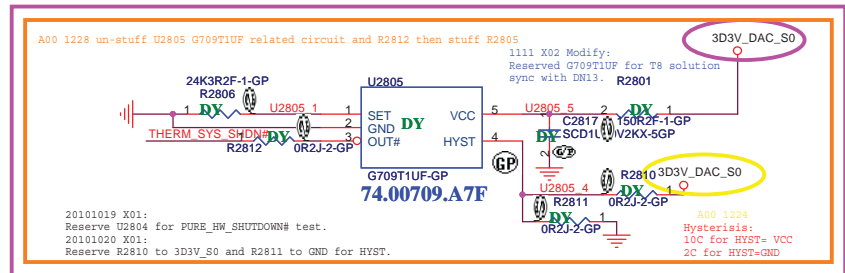
ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101.1
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

EMI/ESD



X02 1111



A00 1228 Cancel VGA Thermal sensor P2800 circuit

1111 X02 Modify:  
ADJ&ADJ\_VGA power source change to 3D3V\_DAC\_S0 from 3D3V\_S0 to solve T8 shut down issue.

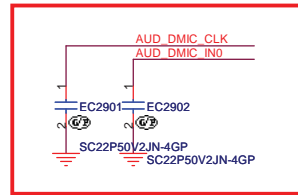
<Core Design>

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# SSID = AUDIO

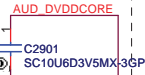
For EMI



1122 X02 Modify:  
change R2920, R2921 to 22ohm from 0ohm and  
stuff R2901, R2902 22p from BNC Neo updated.

27 AMP\_MUTE# >>> AMP\_MUTE#

Close to codec

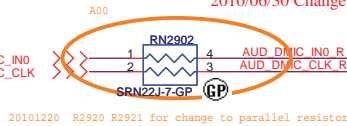


AUD\_DMIC\_CLK\_R  
AUD\_DMIC\_INO\_R  
HDA\_CODEC\_SDOOUT  
HDA\_CODEC\_BITCLK  
HDA\_CODEC\_SDOIN  
HDA\_CODEC\_SYNC  
HDA\_CODEC\_RST#  
AUD\_PC\_BEEP

0707 Modify:  
updated U2901 part number from data base.

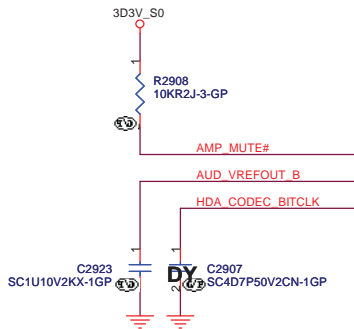
92HD87B1A5NDGXTB8-GP

2010/06/30 Change to 92HD87 (71.92H87.A03)



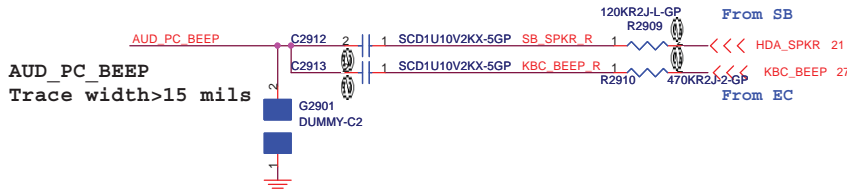
49 AUD\_DMIC\_INO  
49 AUD\_DMIC\_CLK

20101220 R2920 R2921 for change to parallel resistor

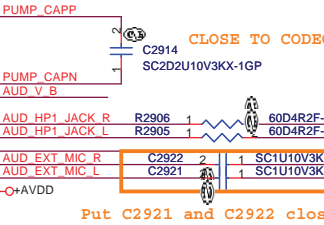
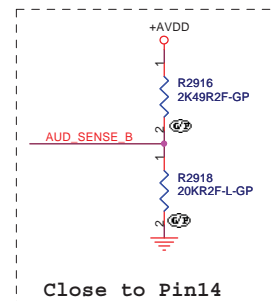
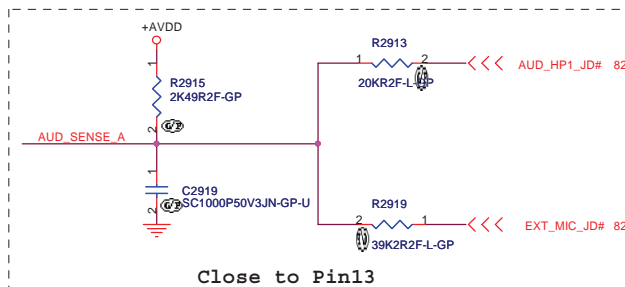
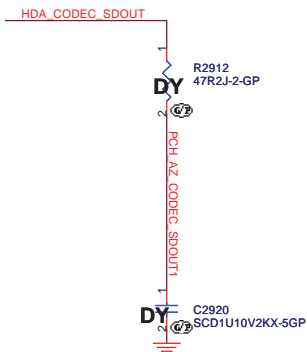


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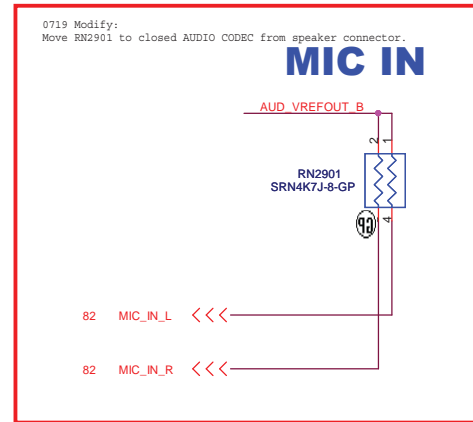
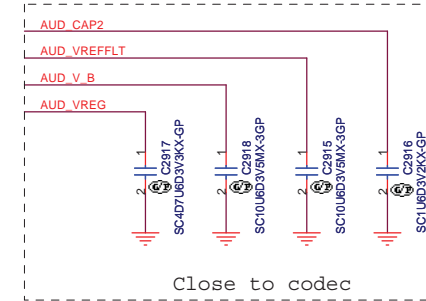
AUD\_PC\_BEEP  
Trace width>15 mils



Azalia I/F EMI



0707 Modify:  
Change R2911, R2914, R2917 change  
to 0ohm 0603 from short pad.  
0726 Modify:  
Removed all of AUD\_AGND and R2911, R2914, R2917.



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Title

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Size  
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QUEEN 15

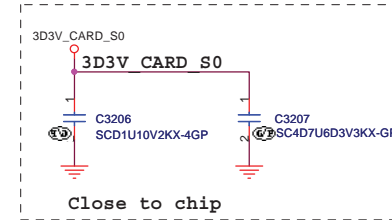
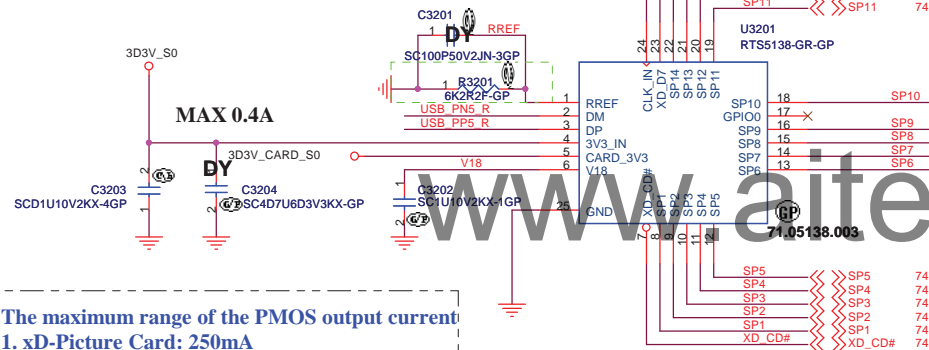
Rev  
A00

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**SSID = SDIO**

48MHz clock input trace of characteristic impedance ( $Z_0$ ) must be 50  $\Omega$   $\pm$  15%.

20 CLK\_PCH\_48M >>>  
PCH GPIO67(48M) confirm with SW

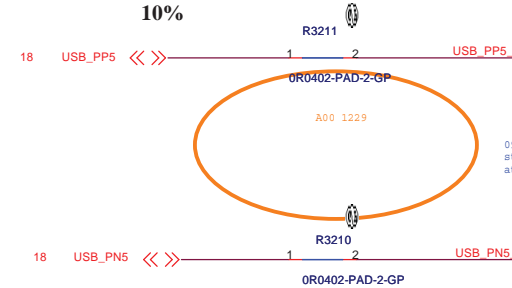


The maximum range of the PMOS output current  
1. xD-Picture Card: 250mA  
2. SD/MMC Card: 250mA  
3. MS/MSPRO/Duo-HG: 250mA

#### POWER TRACE

1. RTS5138: pin 4 (3V3\_IN) trace fixed width is 30 mils (minimum).
2. RTS5138: pin 5 (CARD\_3V3) trace fixed width is 30 mils (minimum).
3. RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum).  
Keep the trace routing lengths as short as possible.
4. RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5. RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6. De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
7. It is recommended that use of ferrites bead on power trace.
8. Via size: Pad>=32 mils, Finished hole>=16 mils.

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance ( $Z_{diff}$ ) is 90 $\Omega$   $\pm$  10%



0917 X01 Modify:  
stuff TR3201 and un-stuff R3211, R3210  
at X01 stage from EMC Neo suggestion.


<Core Design>

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Title: <b>Card Reader-RTS5138</b>			
Size: A3	Document Number: <b>QUEEN 15</b>	Rev: <b>A00</b>	
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Title

**Reserved**


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SSID = Reset.Suspend

## Power Sequence

## ROSA Run Power

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1.5V\_RUN for VGA Consumption  
Peak current 7.39A

+1.5V\_RUN\_CPU Consumption  
Peak current 3A

+1.5V\_RUN for Mini-Card Consumption  
Peak current 1A

5V\_S0

+5V\_RUN Consumption  
Peak current 7.73A

3D3V\_S0

+3.3V\_RUN Consumption  
Peak current 8.14A

1D5V\_S0

MAX Current ? mA  
Design Current ? mA  
Total= 11.39A

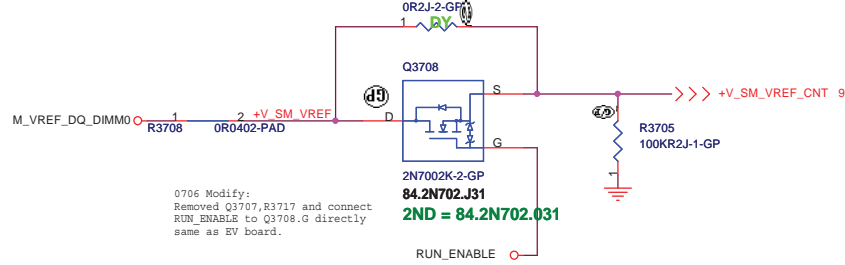
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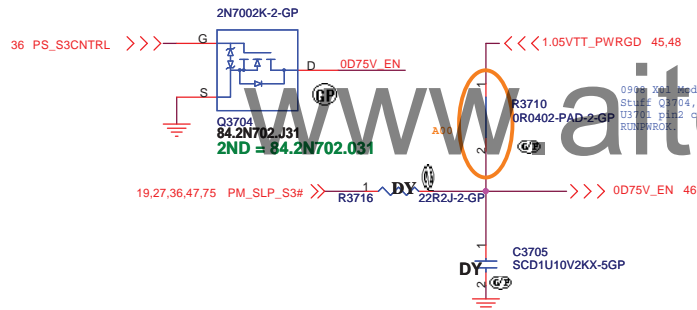
Power Plane Enable			
Size A3	Document Number	QUEEN 15	
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**Close to CPU**  
**S3 Power Reduction Circuit Processor VREF\_DQ Implementation**



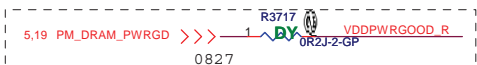
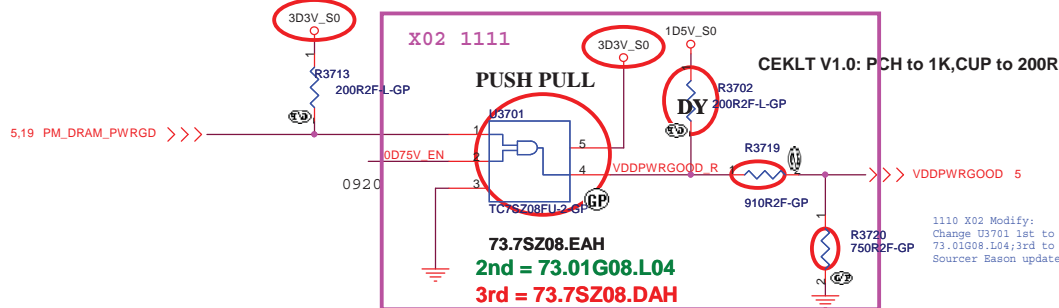
**5 S3 Power Reduction X01 20091111**

0730



0709 Modify:  
Change U3701 pin1,5 to 3D3V\_S0 from 3D3V\_S5.

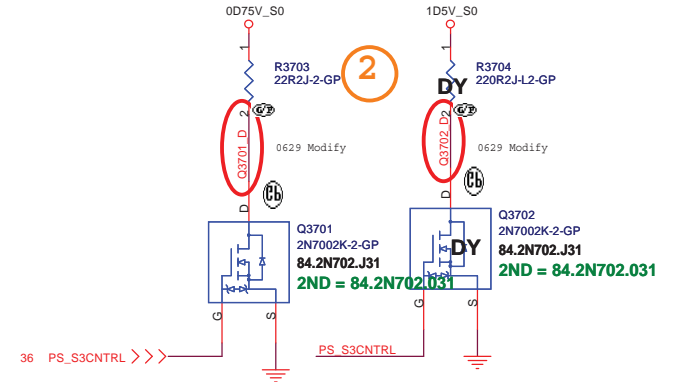
**Close to CPU**  
**S3 Power Reduction Circuit SM\_DRAMPWROK**



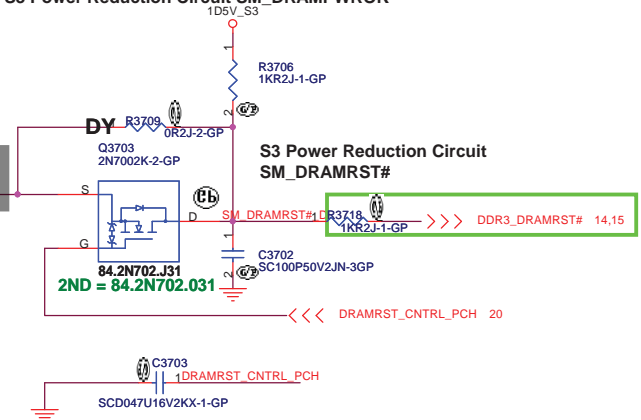
SM DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ \* 0.55; 200mV and the edge must be monotonic

0709 Modify:  
U3701 change to OD type 73.01G09.AAH.  
0723 Modify:  
Change U3701 to push pull type 73.01G08.L04.  
R3720 change to 910ohm 0402.  
R3719 change to 750ohm 0402.  
default un-stuff R3702.

**Close to DIMM**  
**S3 Power Reduction Circuit SM\_DRAMPWROK**



**Close to CPU**  
**S3 Power Reduction Circuit SM\_DRAMPWROK**



DN15ATI


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Title	<b>ADAPTER</b>		
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SSID = PWR.Support

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<Core Design>



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Title

Size

**A3**

Document Number

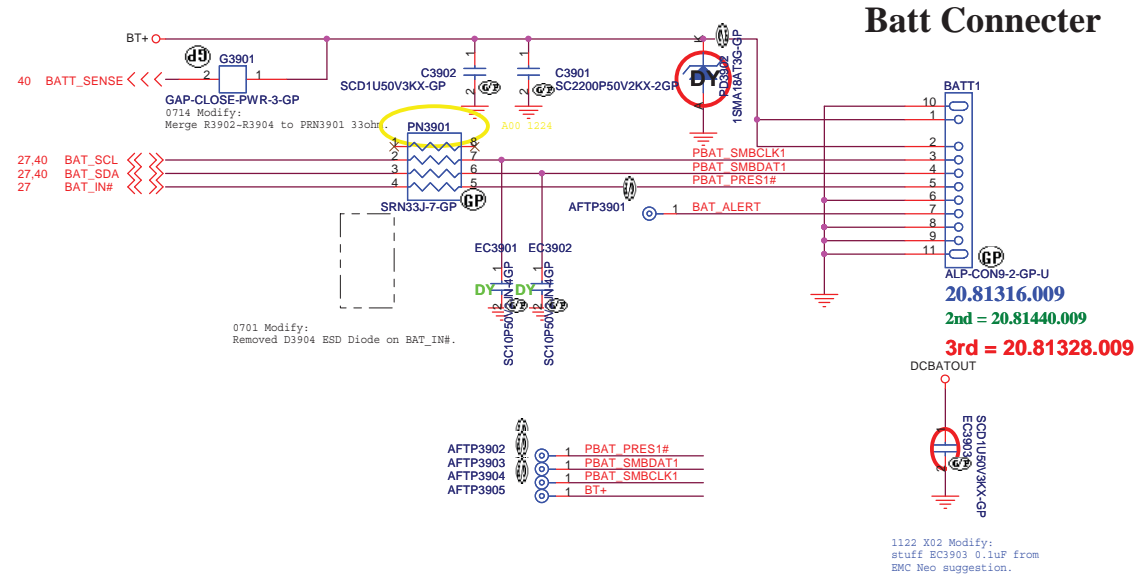
**QUEEN 15**

Rev

**A00**

Date: Tuesday, January 04, 2011

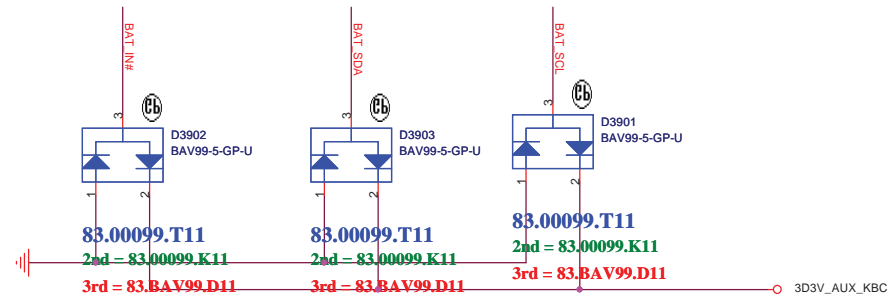
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For actual location, need to be swap all pin

Close to Batt Connector



0930 X01 Modify:  
Change D3901-D3903 main source to 83.00099.T11  
for 83.BAV99.D11 shortage issue.

<Core Design>

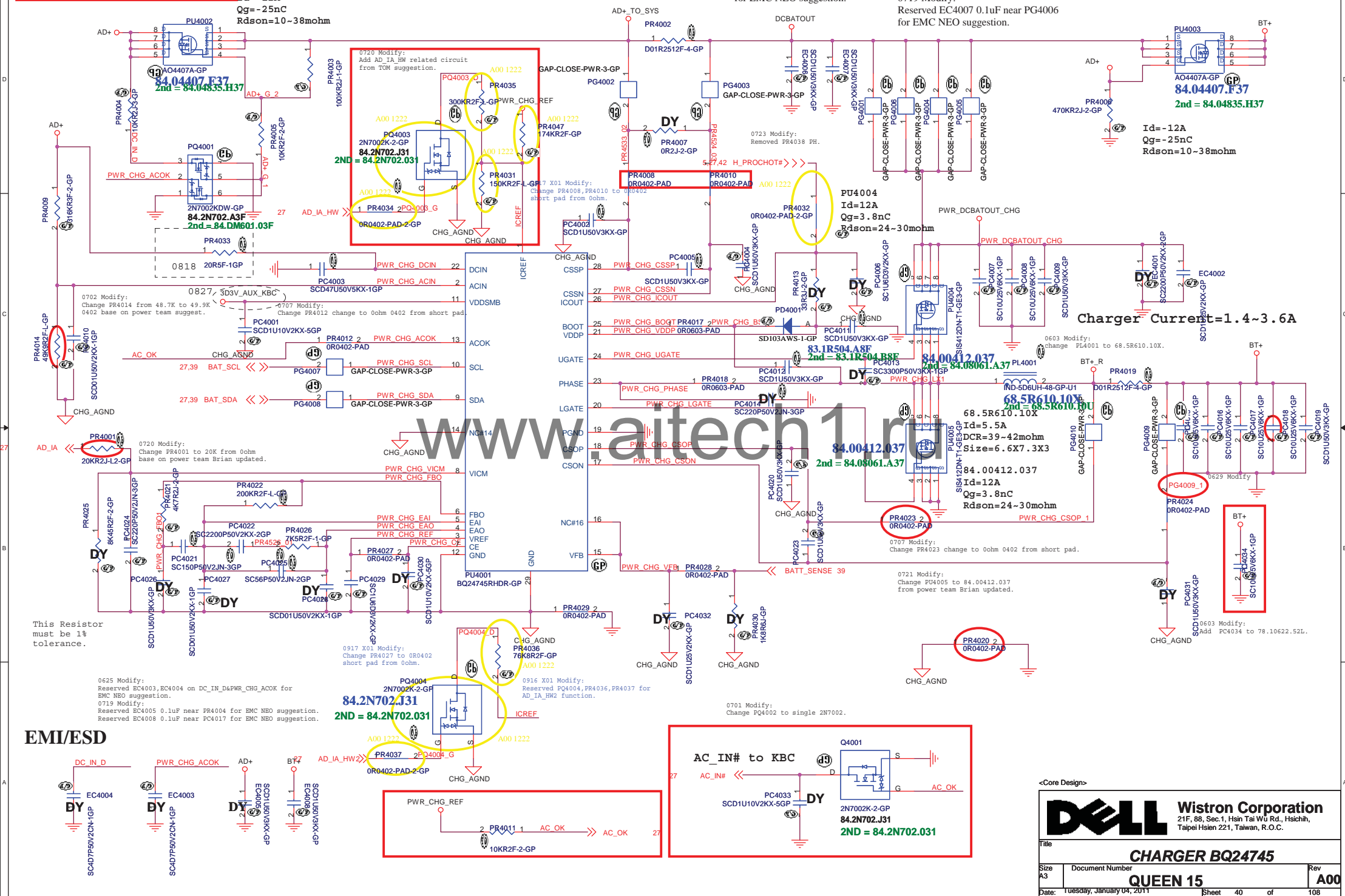
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>BATT CONN</b>			
Size	Document Number	Rev	
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SSID = Charger

Id=-12A  
Qg=-25nC  
Rdson=10~38mohm

0719 Modify:  
Reserved EC4006 0.1uF near PR4002  
for EMC NEO suggestion.

0719 Modify:  
Reserved EC4007 0.1uF near PG4006  
for EMC NEO suggestion.



## EMI/ESD

&lt;Core Design&gt;

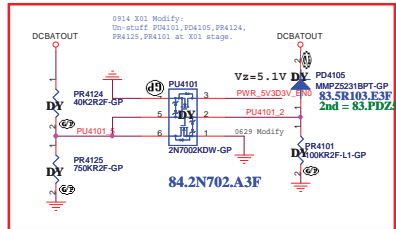
DELL

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Title			
<b>CHARGER BQ24745</b>			
Size A3	Document Number		Rev
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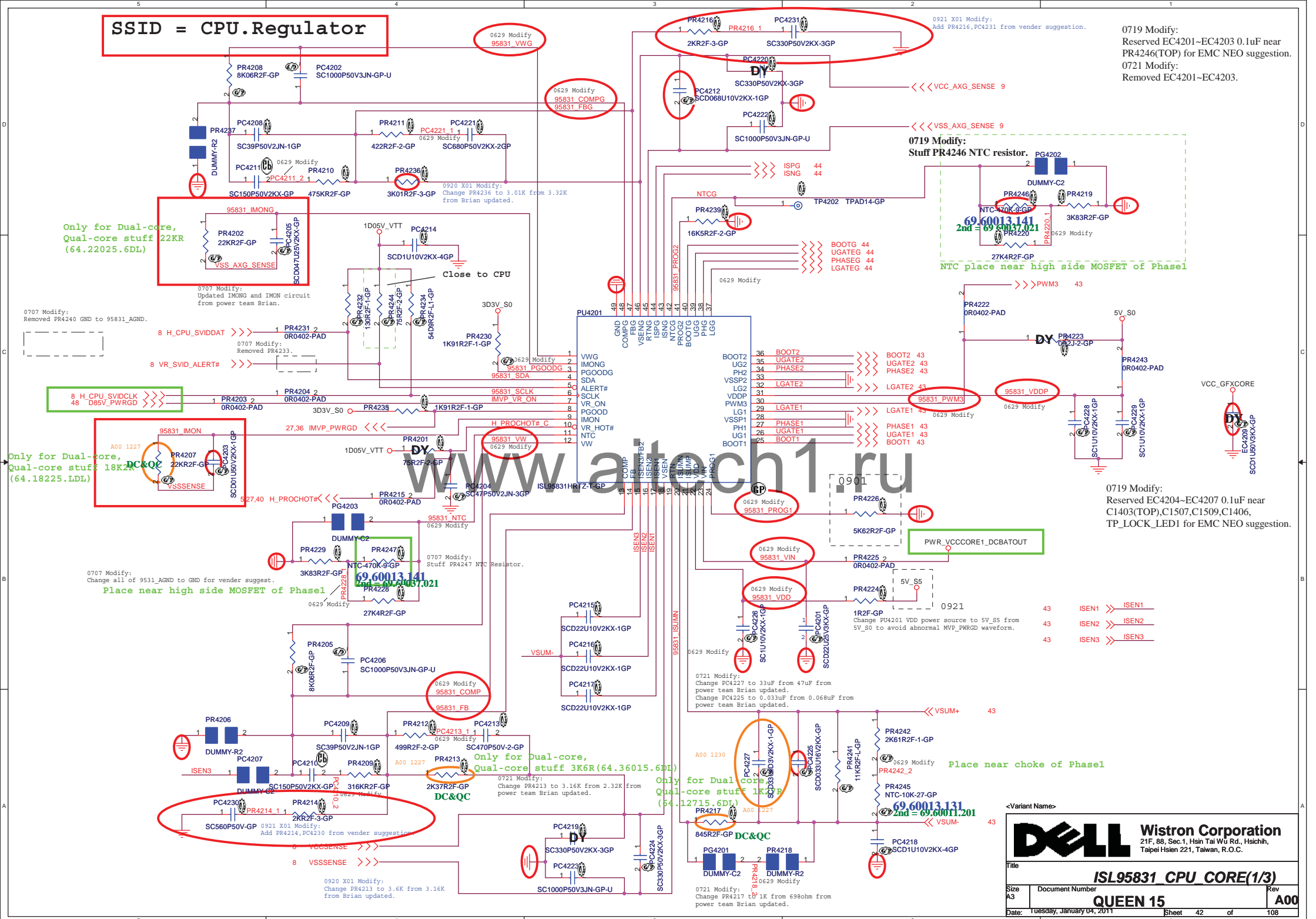


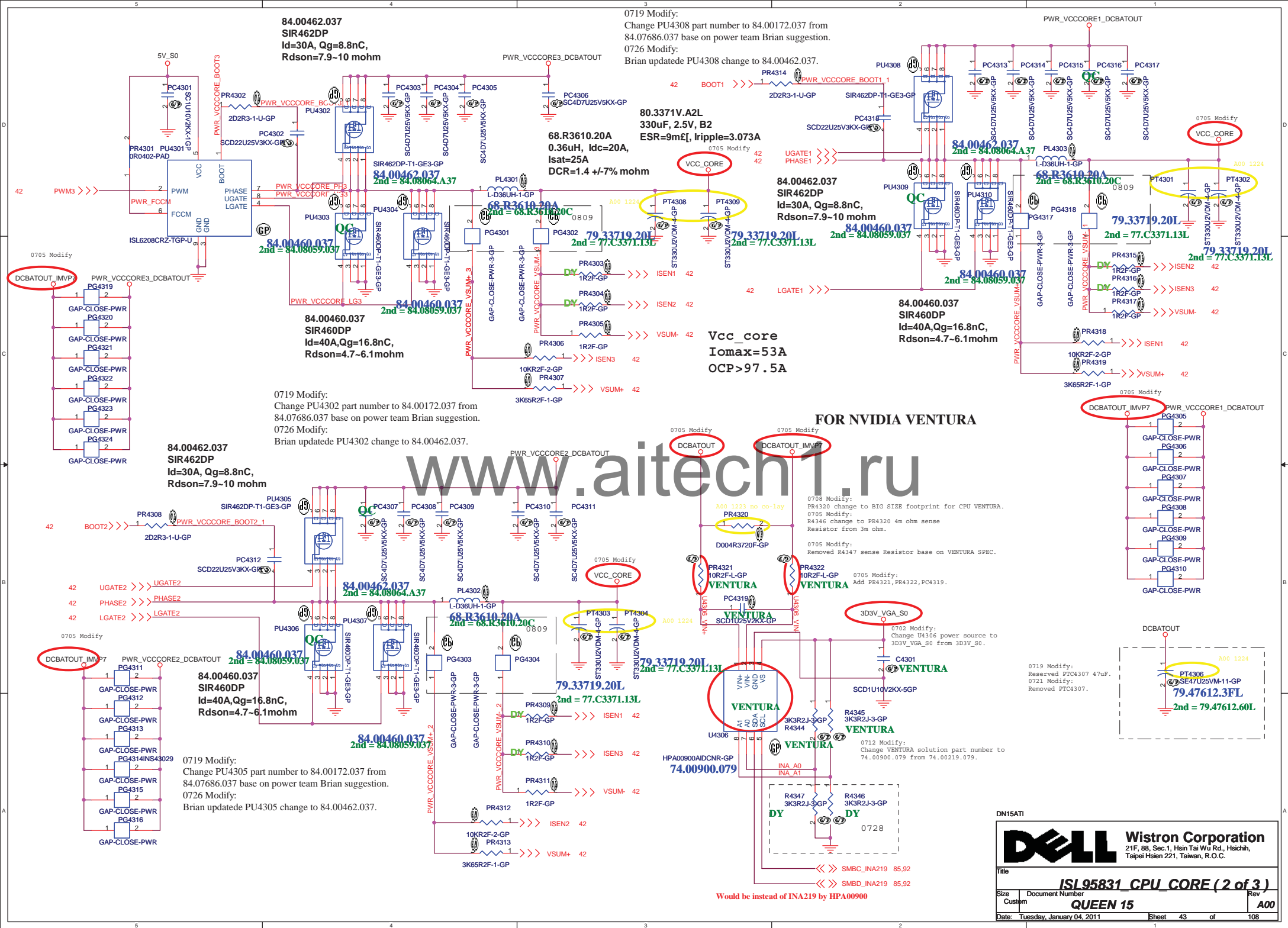
```
SSID = PWR.Plane.Regulator 5v3p3v
```



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

&lt;Variant Name&gt;









1122 X02 Modify:  
stuff EC4501 0.1uF from  
EMC Neo suggestion.



TPS51218 +1.05V VTT

**QUEEN 15**

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SSID = PWR.Plane.Regulator\_1p5v0p75v

0719 Modify:  
Change PU4602 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.

84.00172.037  
BSZ115N03MSC  
Id=20A, Qg=9.8nC,  
Rdson=8.9 mohm

84.00460.037  
SIR460DP-T1-GE3  
Id=40A, Qg=16.8nC,  
Rdson=4.7~6.1 mohm

68.R6810.20G  
68.R6810.20G  
Id=22~39A  
DCR=2.4~2.7mohm  
Size=10X11.5X4

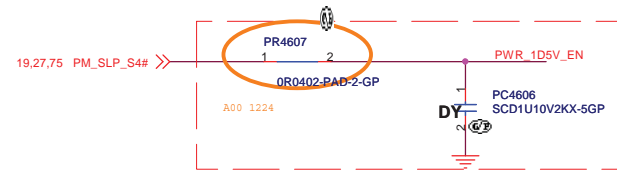
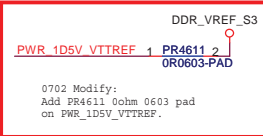
84.00460.037  
2nd = 84.08059.037

Design Current = 14.45A  
22.71A<OCP< 26.84A

79.3971V.30L  
390uF, 2.5V, 6.3X5.7  
ESR=10mΩ, Iripple=3.87A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR5003	400kHz	Tracking Discharge
200k ohm	300kHz	
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

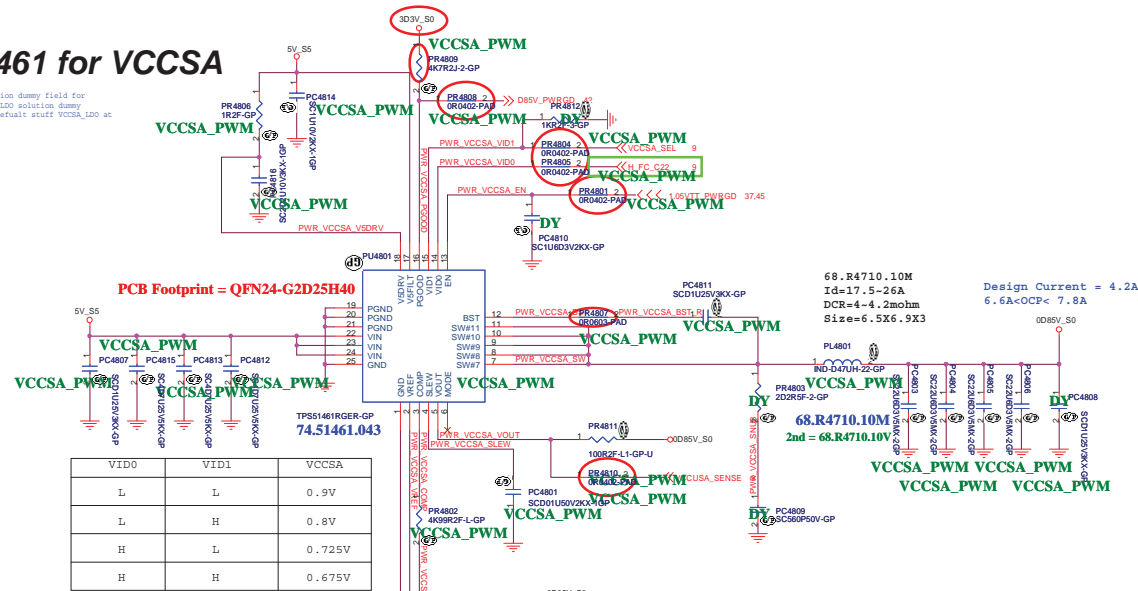






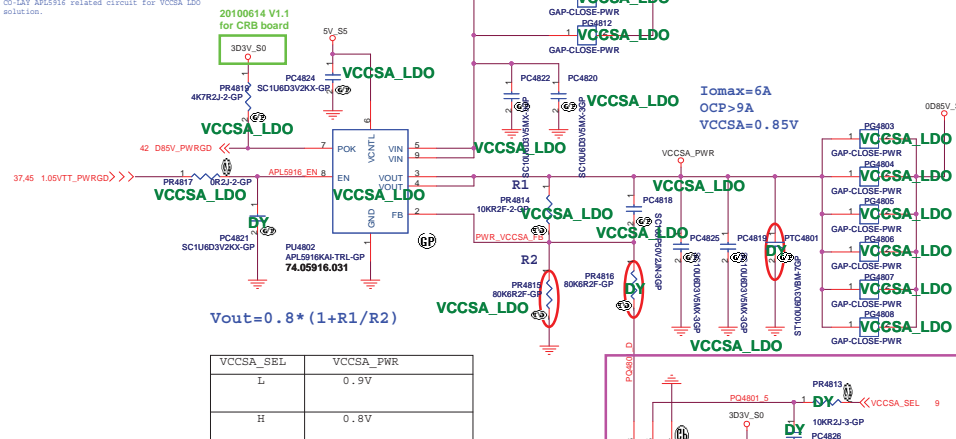
## TPS51461 for VCCSA

1112 X02 Modify:  
set T9B1461 PWM solution dummy field for  
VCCSA\_PWM and APL5916 LDO solution dummy  
field for VCCSA\_LDO. default stuff VCCSA\_LDO at  
ST stage.



## APL5916 for VCCSA

1112 X02 Modify:  
CO-LAY APL5916 related circuit for VCCSA LDO  
solution.



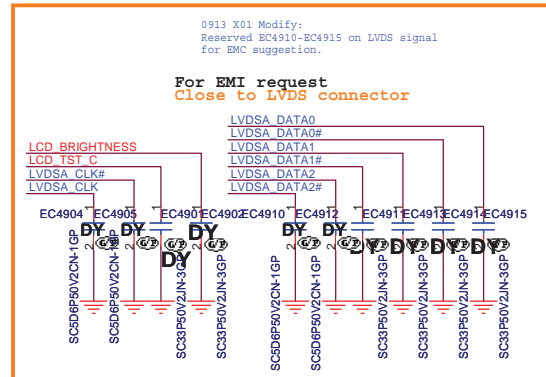
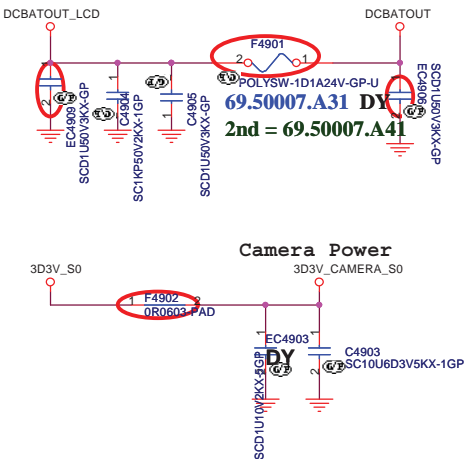
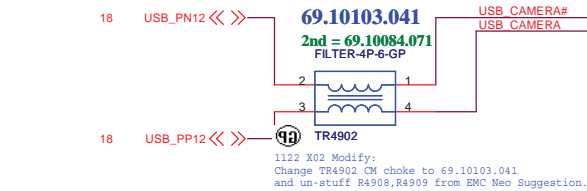
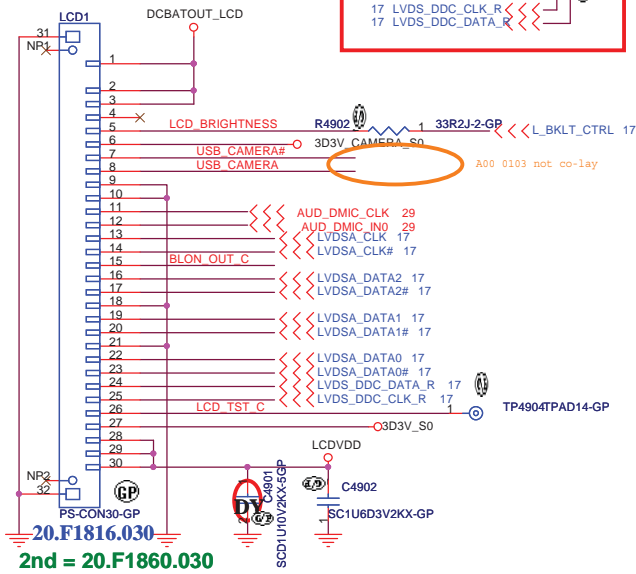
1112 X02 Modify:  
Change PTC4801 to 100u(77.21071.07L)  
from 150u from power team Brian updated.  
1112 X02 Modify:  
Updated VCCSA\_LDO circuit from Power  
team Brian updated.

<Core Design>

# SSID = VIDEO

0909 X01 Modify:  
Change LCD1 to 20.F1816.030 for 30pin  
Re-assign LCD1 pin define base on Roy updated  
cable pin define list.

## LVDS CONNECTOR



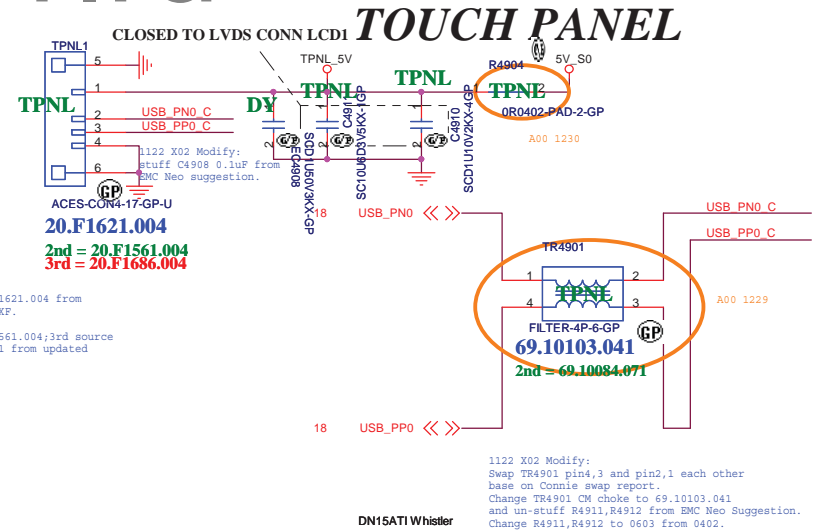
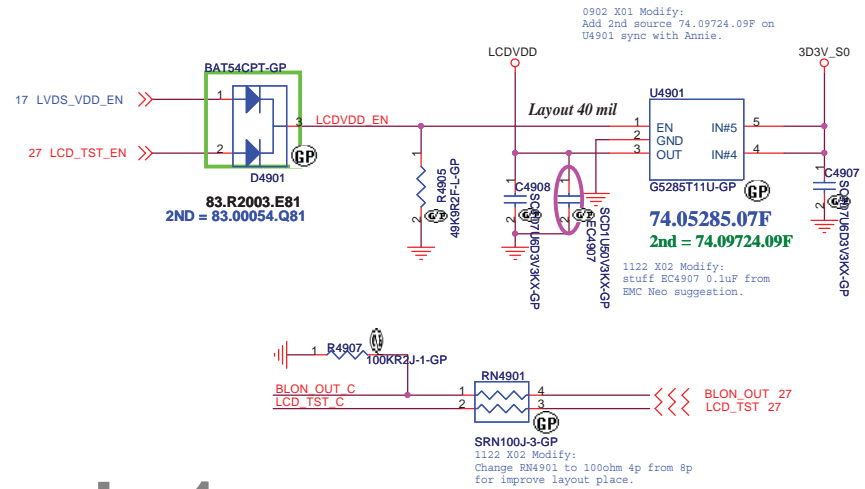
## (MB Pin Define)

### MB CONN. (WIRE)

Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	NC
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	BLON_OUT_C
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD

# SSID = VIDEO

## LCD POWER for ROSA




DN15ATI Whistler

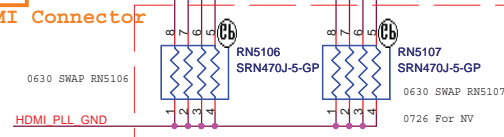
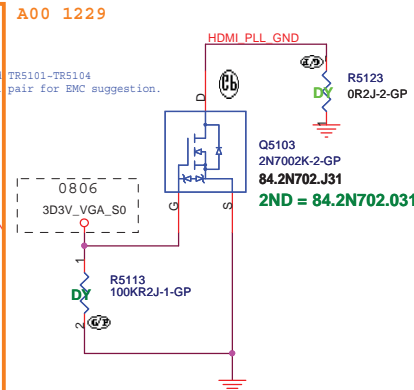
		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>LCD Connector</b>			
Size	Document Number	Rev	
A3	<b>QUEEN 15</b>	<b>A00</b>	
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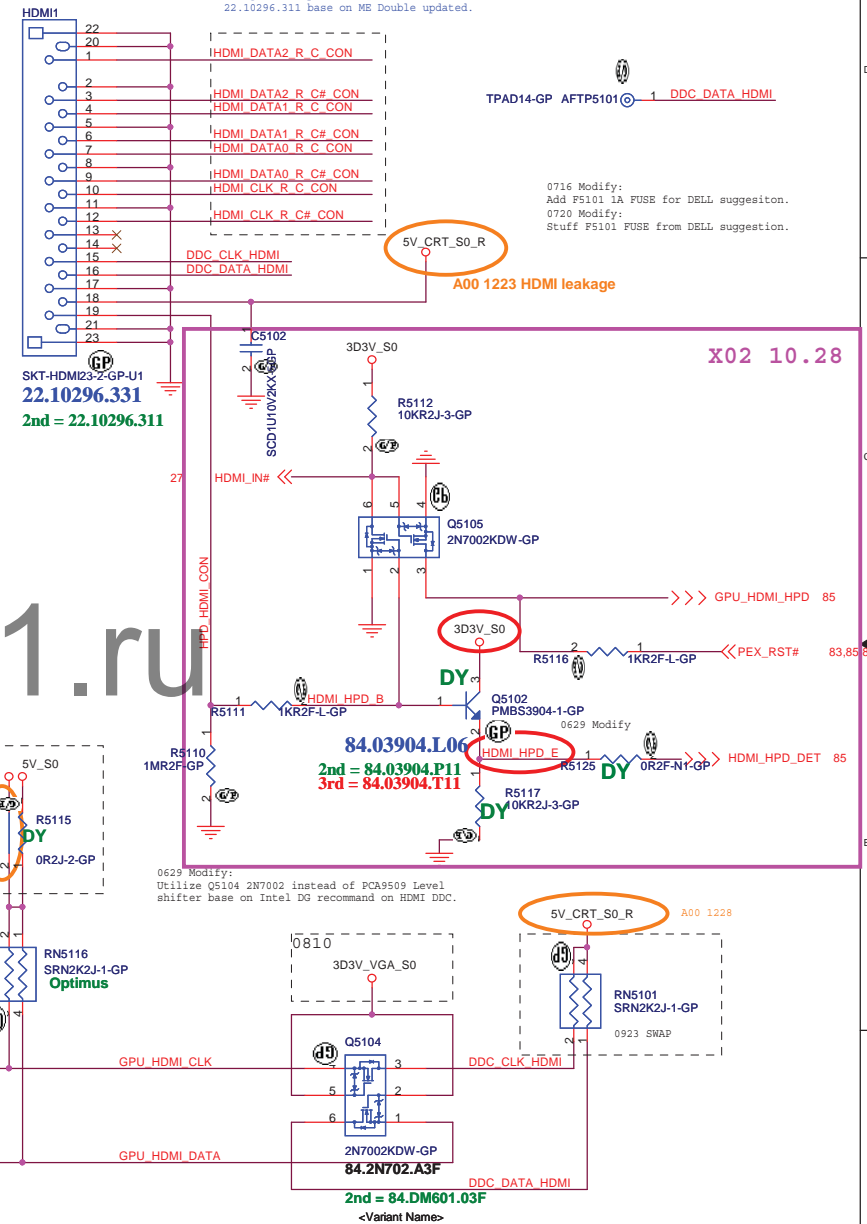
<Variant Name>

		<b>Wistron Corporation</b> <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
<b>CRT Connector</b>			
Size	Document Number		Rev
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## HDMI Level Shifter & CONNECTOR



HDMI CONN



0831 X01 Modify:  
Change HDMI1 part number to 22.10296.311 from  
22.10296.271 base on ME Double updated.  
0910 X01 Modify:  
Change HDMI1 part number to 22.10296.331 from  
22.10296.311 base on ME Double updated.

```
0716 Modify:
Add F5101 1A FUSE for DELL suggesiton.
0720 Modify:
Stuff F5101 FUSE from DELL suggestion.
```

## A00 1223 HDMI leakage

x02 10.28

0629 Modify:  
Utilize Q5104 2N7002 instead of PCA9509 Level  
shifter base on Intel DG recommend on HDMI DDC

2nd = 84.DM601.03F  
<Variant Name>




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<Core Design>



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Title

*Reserved*

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<Core Design>



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Title

**LVDS Switch**


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Title

*Reserved*

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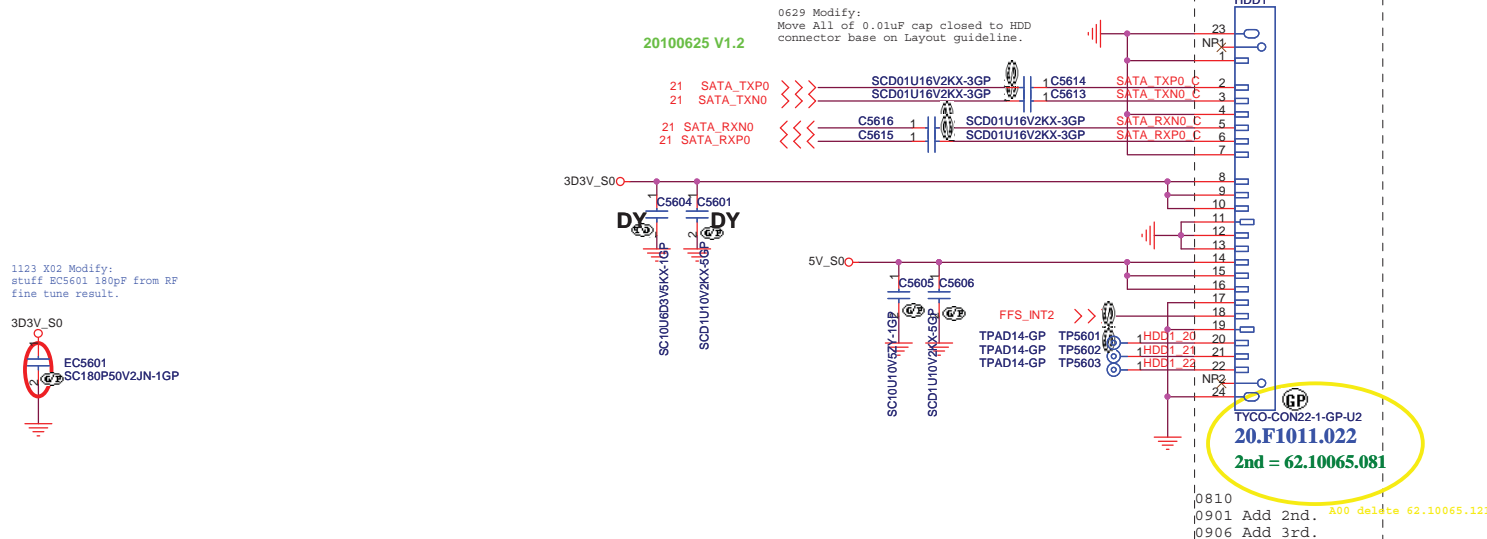
SSID = User.Interface

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SSID = SATA

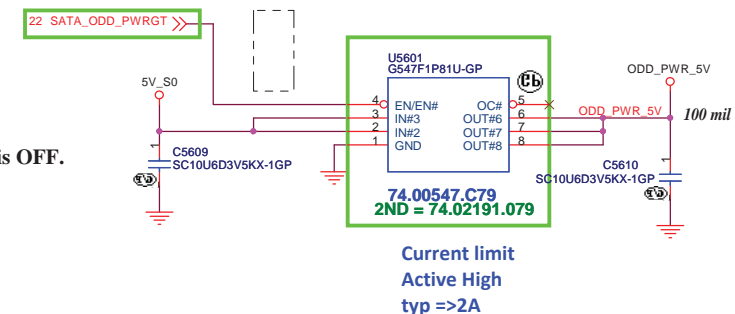
# SATA HDD Connector



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## SATA Zero Power ODD

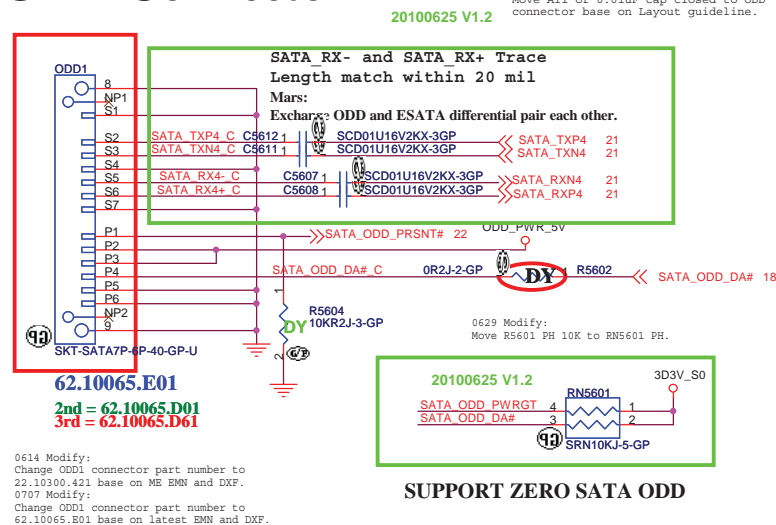
0629 Modify:  
Move R5601 PH 10K to RN5601 PH.



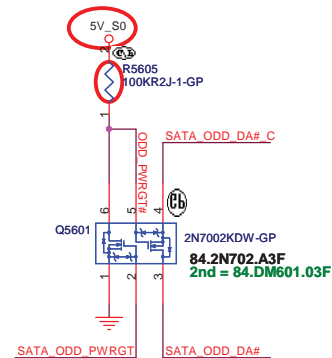
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>HDD/ODD</b>			
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## ODD Connector



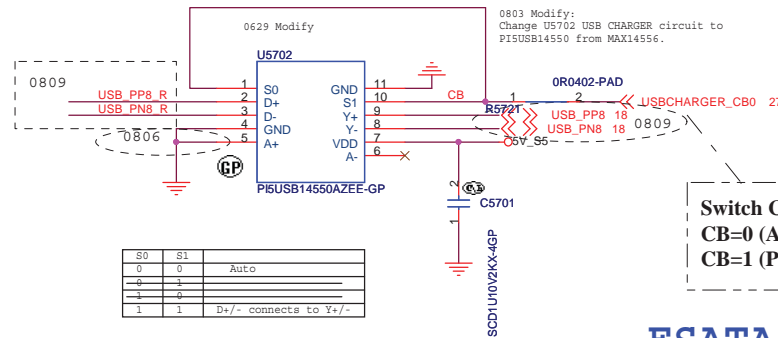
When the drive is powered on, the FET to the MD/DA pin drive is OFF.  
When the drive is powered off, the FET to the MD/DA pin is ON



0707 Modify:  
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SSID = ESATA

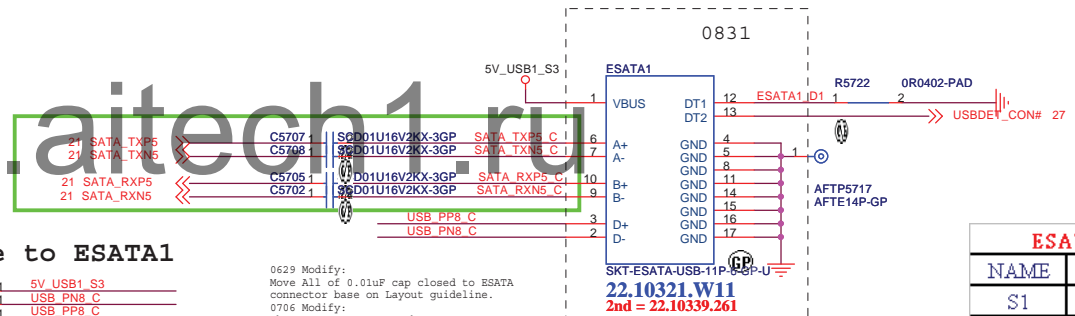
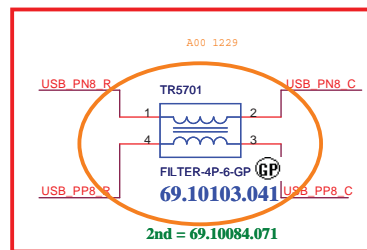
## USB CHARGER



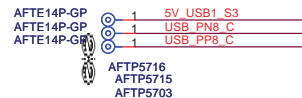
**Switch Control Bit:**

**CB=0 (AM):**auto detection charger identification active.  
**CB=1 (PM):**connect DP/DM to TDP/TDM.

**ESATA CONN**



close to ESATA1



```
0629 Modify:
Move All of 0.01uF cap closed to ESATA
connector base on Layout guideline.
0706 Modify:
Change ESATA part number to 22.10321.F71
base on latest EMN and DXF.
0713 Modify:
Add USBDET_CONN on ESATA pins for
USB to SATA detect solution. ESATA_CONN
should be searched for detect type connector.
0719 Modify:
ME Double provide temporary foxconn ESATA conn
22.10290.141 for SSI stage function test.
```

### E-SATA USB 2.0 Combo

**CE/H=-0.16/2.83mm with detect function**

ESATA	
NAME	TYPE
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
USB	
NAME	TYPE
U1	VBUS
U2	D-
U3	D+
U4	GND

## <Core Design>



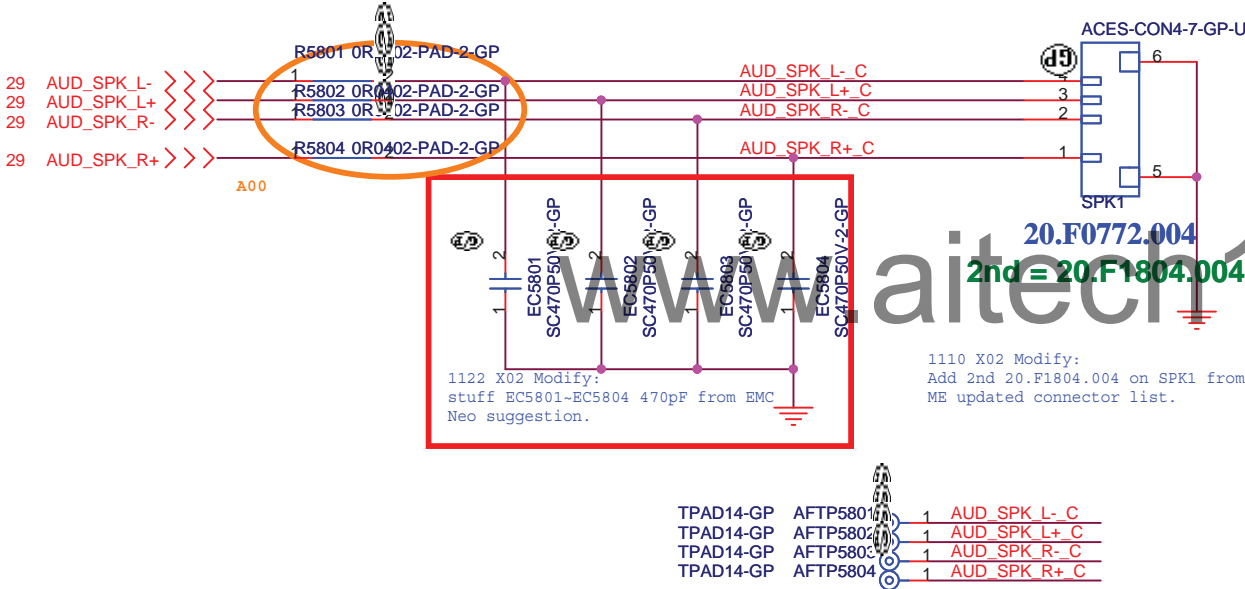
**Wistron Corporation**  
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Title **ESATA**

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SSID = AUDIO

Speaker Connector



MB CONN. (WIRE)	
Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

0913 X01 Modify:  
Change SPK1 to 20.F0772.004 from  
20.F1647.004 from Double updated.  
0914 X01 Modify:  
Re-assign SPK1 pin define base on  
Roy updated excel file for 20.F0772.004

1110 X02 Modify:  
Add 2nd 20.F1804.004 on SPK1 from  
ME updated connector list.

<Core Design>



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Title

**SPEAKER CONN**

Size  
A4

Document Number  
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Rev  
**A00**

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Title

**Reserved**

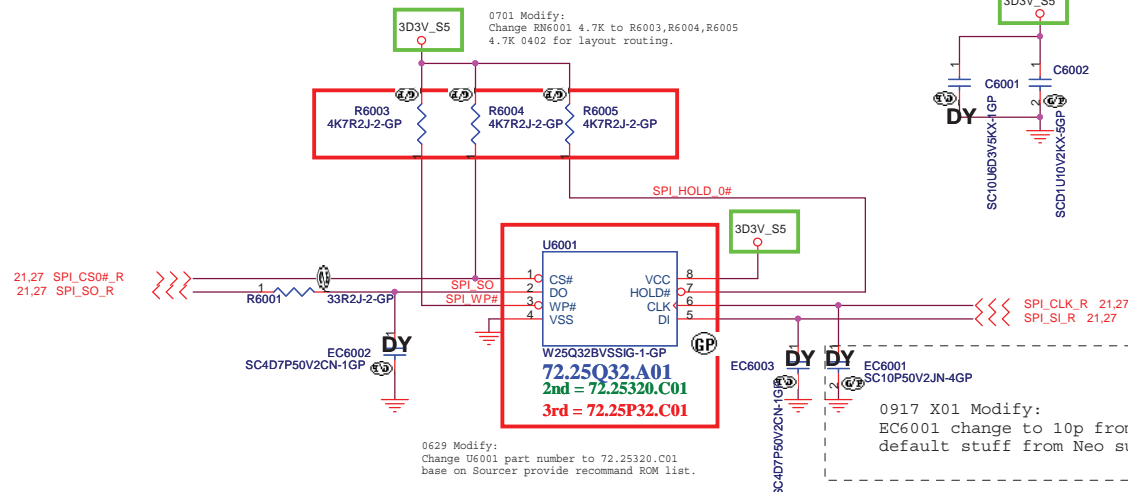
Size	Document Number	Rev
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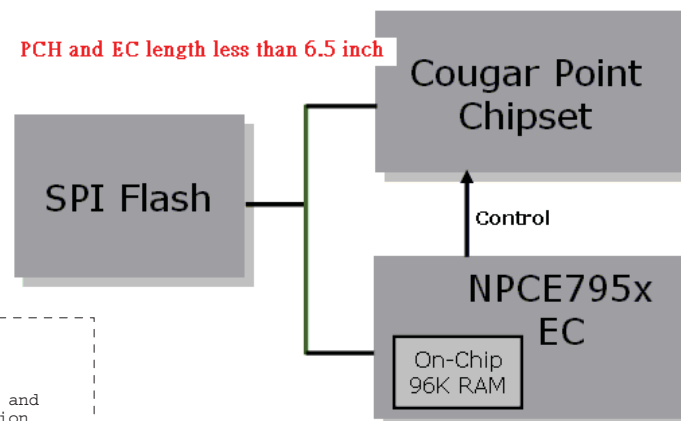
SSID = Flash.ROM

## SPI FLASH ROM (4M byte) for PCH



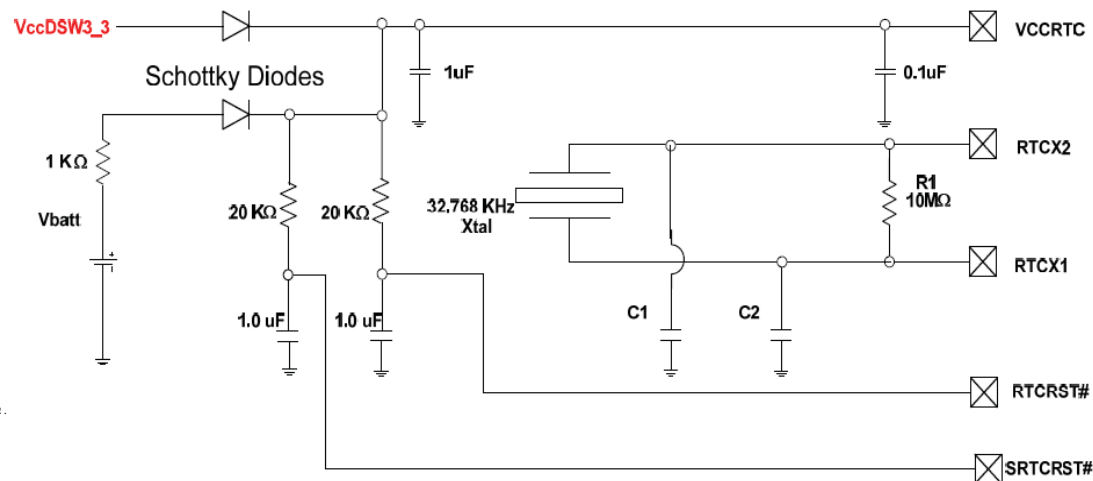
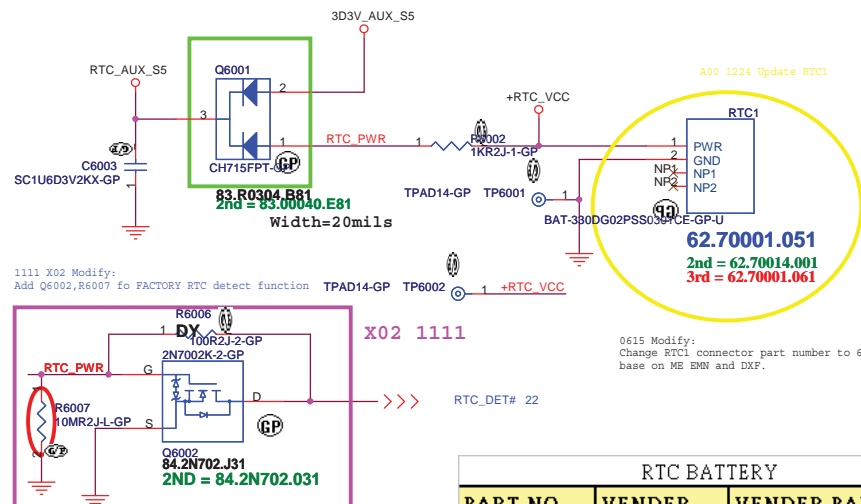
Notes:  
The total SPI interface signal between EC and PCH  
can't not exceed 6500mil. The mismatch between  
SPI signal must be within 500mil

PCH and EC length less than 6.5 inch



Priority	Wistron P/N	Manufacturer	Vendor P/N
X02	1	72.25Q32.A01	WINBOND
	2	72.25320.C01	MXIC
X02	3	72.25P32.C01	Numonyx
			M25BX32-VMW6F

SSID = RBATT



VccRTC is now connected to VccDSW3\_3  
through the Schottky diode instead of the 3.3V Sus well.

RTC BATTERY		
PART NO	VENDER	VENDER PART NO.
23.20023.311	MITSUBISHI	CR2032 MITSUBISHI
23.20023.341	HENSHEN	CR-2032L/DBE
23.20068.001	KTS	BBBCR2032BX

<Variant Name>

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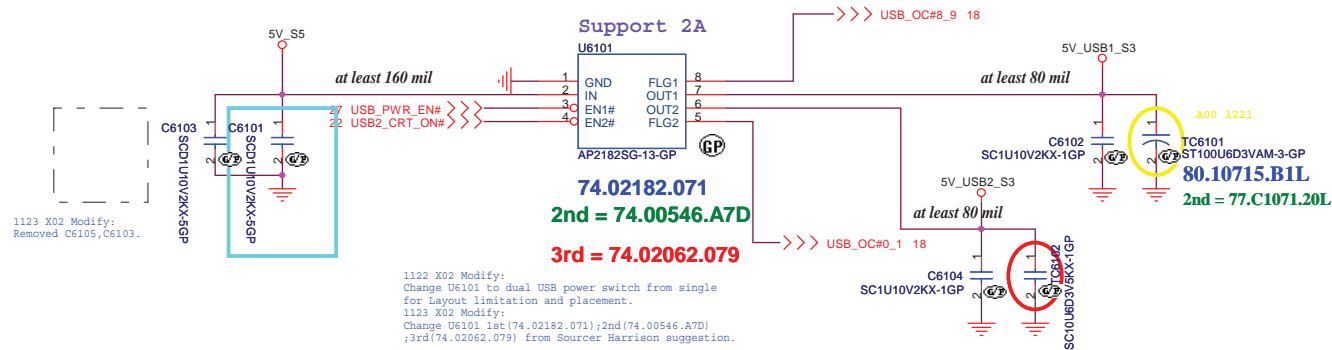
Title: **Flash/RTC**

Size: A3 Document Number: **QUEEN 15** Rev: **A00**

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SSID = USB

## CRT Board and COMBO USB Power



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<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB Power SW</b>			
Size	Document Number		Rev
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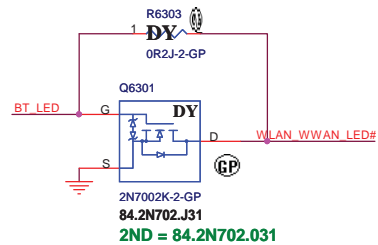
Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

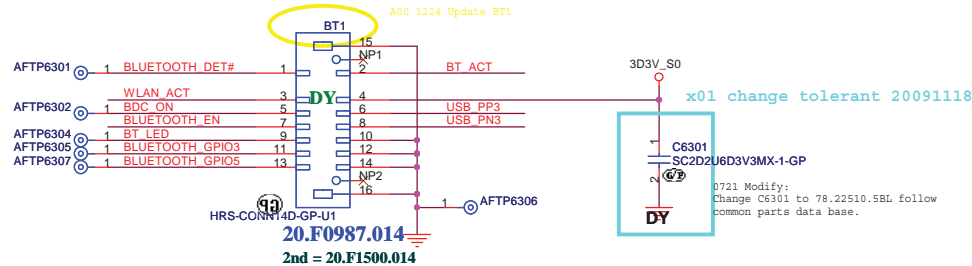
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# SSID = User.Interface

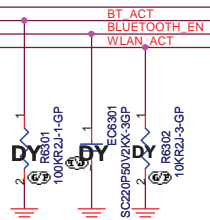


0722 Modify:  
Add Q6301 and combine BT\_LED to  
WLAN\_WWAN\_LED#.

## Bluetooth Module conn.



68.82 WLAN\_WWAN\_LED#  
18 USB\_PP3  
18 USB\_PN3  
82 BT\_ACT  
27.82 BLUETOOTH\_EN  
82 WLAN\_ACT



AFTP6309 1 WLAN\_ACT  
AFTP6310 1 BLUETOOTH\_EN  
AFTP6308 1 BT\_ACT  
AFTP6311 1 3D3V\_S0  
AFTP6312 1 USB\_PP3  
AFTP6313 1 USB\_PN3

0709 Modify:  
PM confirmed there is no stand-alone BT module,  
so DY BT1 connector, add BT enable signal  
and 5V\_S5 power option on WLAN connector pin 51.  
0712 Modify:  
Stuff BT relatek component to verify function.

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Title

**Bluetooth**

Size  
A3

Document Number

**QUEEN 15**

Rev

**A00**

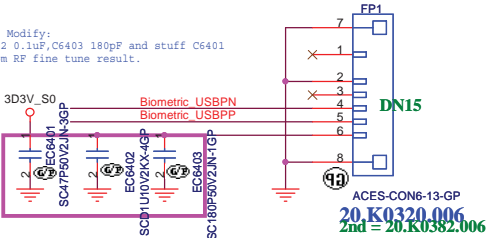
Date: Tuesday, January 04, 2011

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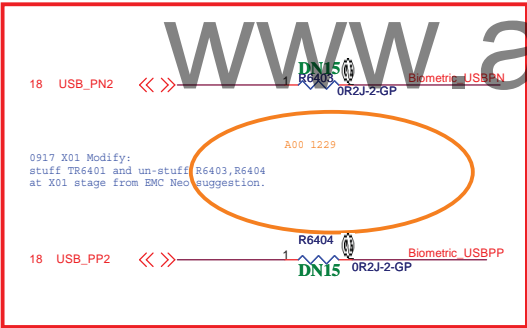
Finger Printer Connector

0707 Modify:  
Add FP\_DET# signal on FP1 pin1.  
0715 Modify:  
Add FP\_DET# signal on FP1 pin1.  
0806 Swap pin.  
0810 Change to 4 pin.  
0827 Change to 6 pin.

1123 X02 Modify:  
Add C6402 0.1uF,C6403 180pF and stuff C6401  
47pF from RF fine tune result.




MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V_S0



0615 Modify:  
Change FP1 connector part number to 20.K0320.004  
base on ME EMN and DXF.  
0630 Modify:  
Change FP1 connector part number to 20.K0320.006  
base on ME EMN and DXF.  
0707 Modify:  
Reassign Figer print pin define base on EXCEL FILE.  
0713 Modify:  
Reassign Figer print pin define base on EXCEL FILE.  
Removed FP\_DET# on FP1.

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Title


**RESERVED**

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<Core Design>



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Title

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Title

**Reserved**

Size	Document Number	Rev
A3	<b>QUEEN 15</b>	<b>A00</b>

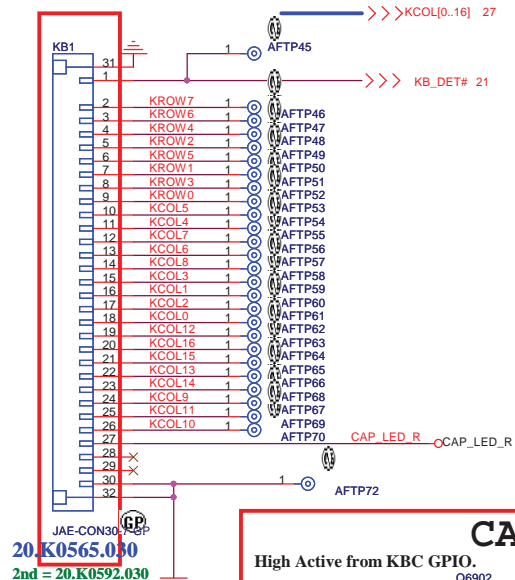
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```
0715 Modify:
Removed PWR_BTN_LED# control circuit
base on Dell feedback.
```

SSID = KBC

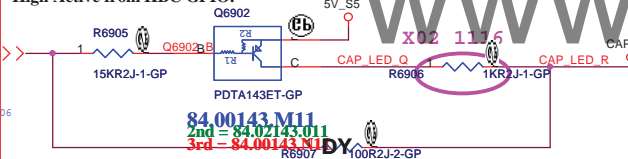
## Internal KeyBoard Connector

0630 Modify:  
Change KB1 part number to 20.K0565.030  
base on ME updated EMN and DXF.

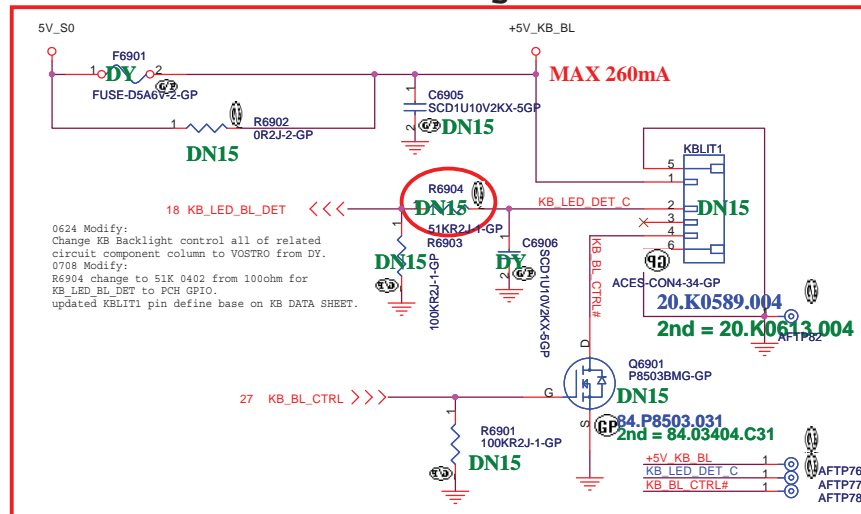


## CAP LED CONTROL

High Active from KBC GPIO.



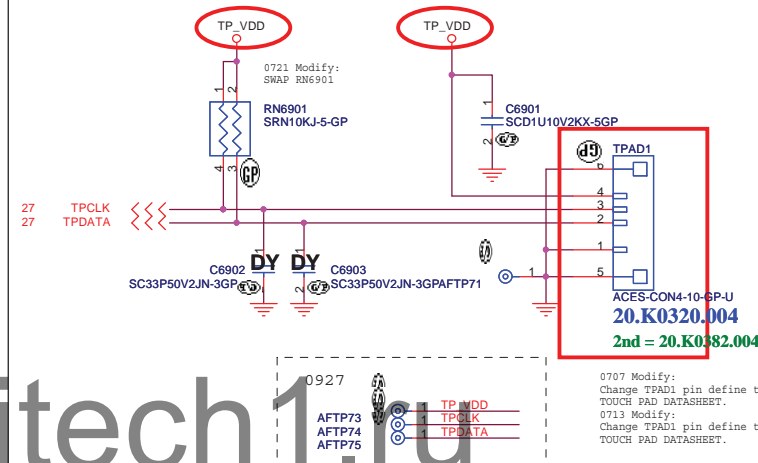
## KB Backlight Connector



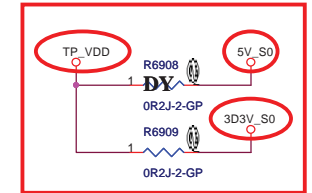
MB Pin	Description
1	Diag_Loop3 = GPIO_1 (TPC)
2	KSII[7] = KBD S8
3	KSII[6] = KBD S7
4	KSII[4] = KBD S5
5	KSII[2] = KBD S3
6	KSII[5] = KBD S6
7	KSII[1] = KBD S2
8	KSII[3] = KBD S4
9	KSII[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	NC (reserved for Caps LK LED)
28	NC (reserved for Num LK LED)
29	NC (reserved for Scroll LK LED)
30	GND

SSID = Touch.Pad

## TouchPad Connector



0715 Modify:  
Add R6908, R6909 for TPAD1 co-lay power option.



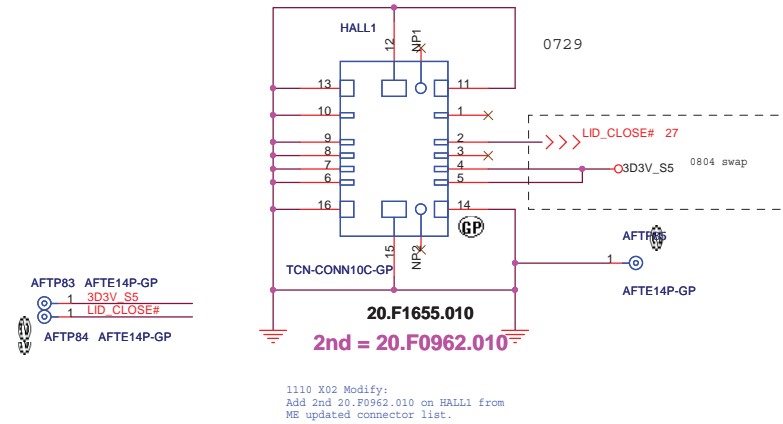
MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

SKEW	OPTION1	OPTION2	PIN	Feature	REMARK
DQ13	C12S		30		S is mean small
DN13	C12S	C12SB	30/25	Backlight	SB is mean small with backlight
DN15	C12S	C12SB	30/25	Backlight	
DQ15	C12SN		30	KB_DET#,CAP LED	SN is mean small with numpad

MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#

0901 X01 Modify:  
Change KBLIT1 to 20.K0320.004 from  
20.K0218.004 base on ME updated X01 DXF&EMN.  
Re-assign KBLIT1 pin define sync with DQ15\_NV.  
0914 X01 Modify:  
Add 2nd source 20.K0382.004 on KBLIT1  
base on updated connector list.  
0923 X01 Modify:  
Change KBLIT1 part number to 20.K0589.004  
and re-assign pin define base on Roy updated.

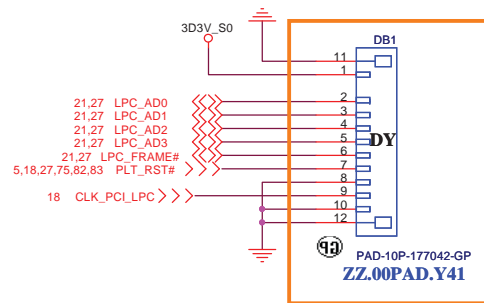
<Core Design>



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<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Hall Sensor</b>			
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A00 122# DB1 change to ZZ.00PAD.Y41 (solder mask type)  
and keep un-stuff at X-Build stage

<Core Design>



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Title

**Dubug connector**

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<Core Design>



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Title

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Title

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Size  
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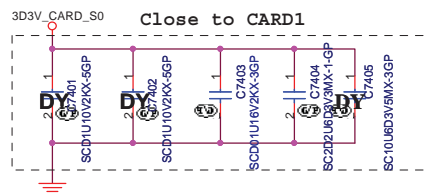
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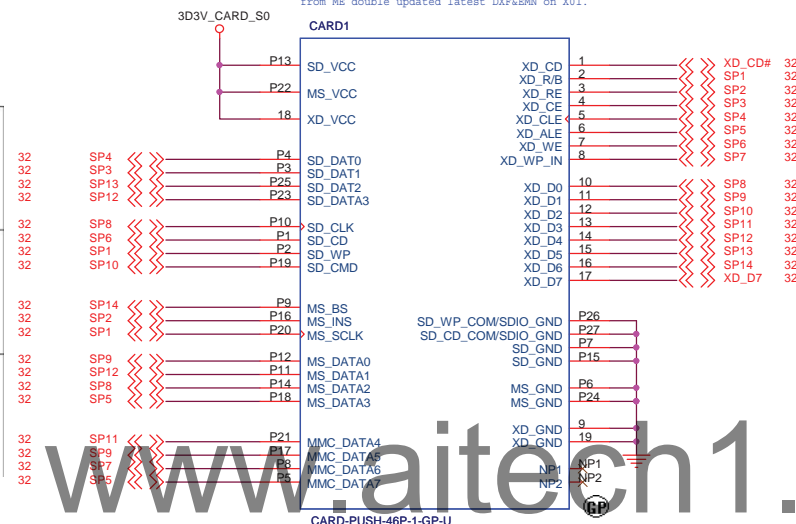


SSID = SDIO



***SD/XD/MS/MMC+ Card Reader***

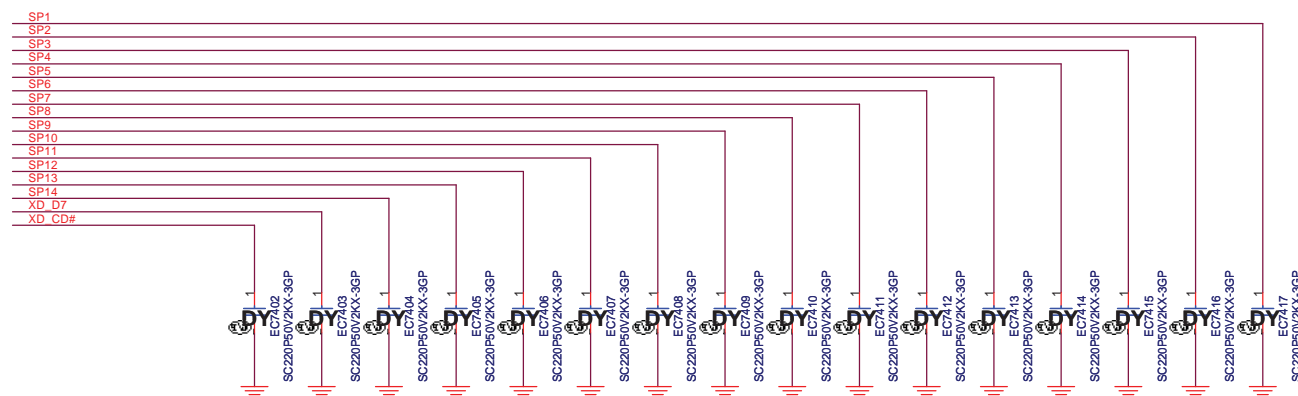
0906 X01 Modify:  
Change CARD1 to 20.10129.001 from 62.10051.931  
from ME double updated latest DXF&EMN on X01.



**20.10129.001**

2nd = 20.10135.001

1119 X02 Modify:  
Add 2nd 20.I0135.001 on HALL1 from  
ME updated connector list.



20.10129.001			
Pin	TYPE	FUNCTION	RTSS138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC_PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC_PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC_PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC_PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM /SDIO GND	GND
P27	SD	SD-CD COM /SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R/B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

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Title

**SD/XD/MS/MMC Card CONN**

Size

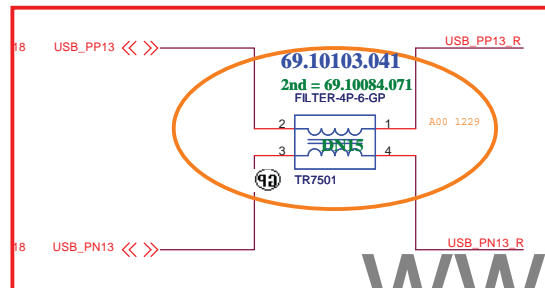
Document Number

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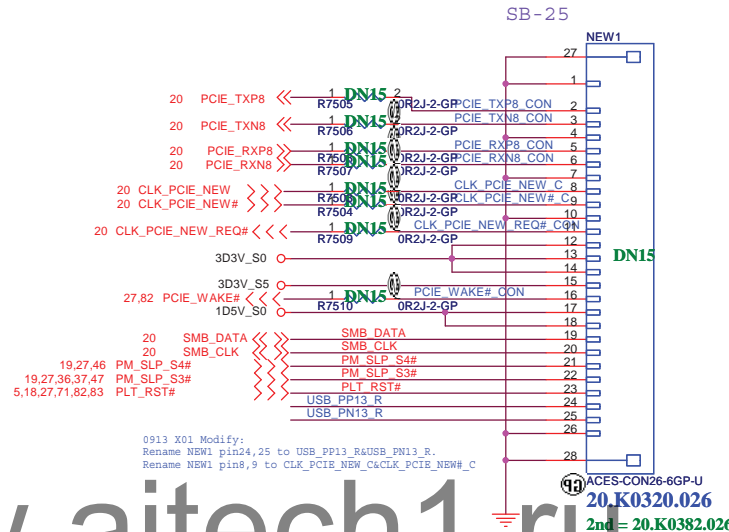
1122 X02 Modify:  
Change TR7501 CN choke to 69.10103.041  
and un-stuff R7501, R7502 from EMC Neo Suggestion.  
Change R7501, R7502 to 0603 from 0402.



AFTE14P-GP AFTP107	1	3D3V_S5
AFTE14P-GP AFTP108	1	3D3V_S0
AFTE14P-GP AFTP109	1	1D5V_S0
AFTE14P-GP AFTP110	1	USB_PN13_R
AFTE14P-GP AFTP111	1	USB_PP13_R
AFTE14P-GP AFTP112	1	CLK_PCIE_NEW_REQ#_CON
AFTE14P-GP AFTP113	1	SMB_CLK
AFTE14P-GP AFTP114	1	SMB_DATA
AFTE14P-GP AFTP115	1	PM_SLP_S3#
AFTE14P-GP AFTP116	1	PM_SLP_S4#
AFTE14P-GP AFTP117	1	PLT_RST#
AFTE14P-GP AFTP118	1	CLK_PCIE_NEW#_C
AFTE14P-GP AFTP119	1	CLK_PCIE_NEW_C
AFTE14P-GP AFTP120	1	PCIE_TXN8_CON
AFTE14P-GP AFTP121	1	PCIE_TXP8_CON
AFTE14P-GP AFTP122	1	PCIE_RXN8_CON
AFTE14P-GP AFTP123	1	PCIE_RXP8_CON
AFTE14P-GP AFTP124	1	PCIE_WAKE#_CON

1D5V\_S0\_CARD Max. 650mA, Average 500mA.  
3D3V\_S0\_CARD Max. 1300mA, Average 1000mA  
3D3V\_S5\_CARDAUX Max. 275mA

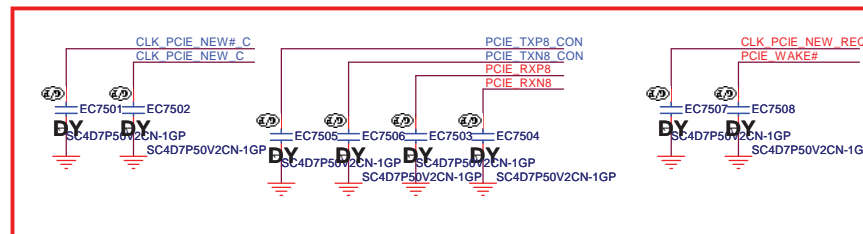
0824 X01 Modify:  
Due to our NEW1 change to Express card to  
bottom side so re-assign NEW1 pin define same  
as DQ15-WY.  
0906 X01 Modify:  
Add 2nd source 20.K0382.026 on NEW1 base on  
updated connector list.



0913 X01 Modify:  
Rename NEW1 pin24,25 to USB\_PP13\_R&USB\_PN13\_R.  
Rename NEW1 pin8,9 to CLK\_PCIE\_NEW\_C&CLK\_PCIE\_NEW#\_C

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For BMT



0913 X01 Modify:  
Add R7503, R7504 and reserved EC7501, EC7502 on  
CLK\_PCIE\_NEW & CLK\_PCIE\_NEW# for EMC suggestion.  
0921 X01 Modify:  
Add R7505-R7508 0ohm and reserved EC7503-EC7506  
on PCIE\_TXP8&TXN signal base on EMC Lance suggestion.  
Add R7509, R7510 0ohm and reserved EC7507, EC7508  
on CLK\_PCIE\_NEW\_REQ#&PCIE\_WAKE# signal base  
on EMC Lance suggestion.

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Express Card		
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Title

**Reserved**


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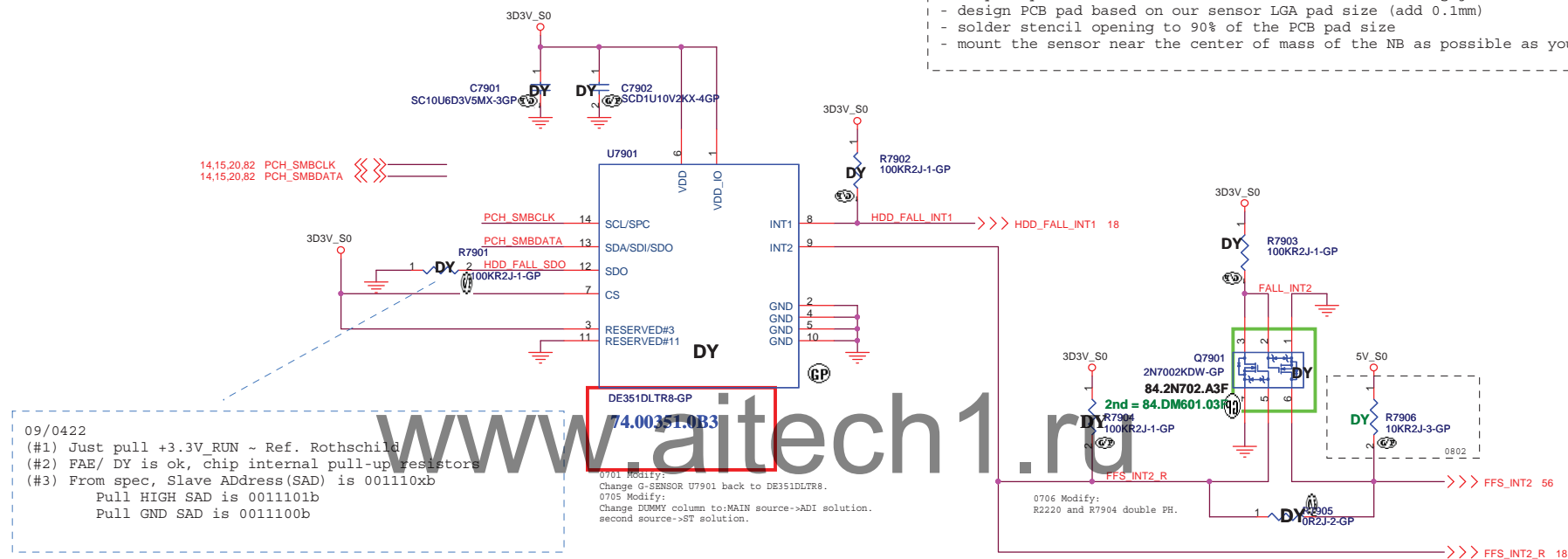
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```
SSID = User.Interface
```

## Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

<Core Design>

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## Free Fall Sensor

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QUEEN 15

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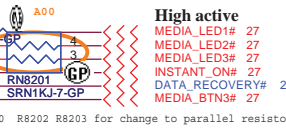
Rev  
A00

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Board CONN 80 pin  
 1112 X02 Modify:  
 Dell required us to disable PCIE port of WWAN slot  
 ,if PCIE port 1 is disabled, it will cause all PCIE port  
 disabled,so change WWAN to PCIE port 3 from port1  
 at ST stage.



```
0906 X01 Modify:  
Add 2nd source 20.F0085.040 on CRTBD1  
base on updated connector list.  
0915 X01 Modify:  
Re-assign CRTBD1 pin define base on  
EMC suggestion.
```



## <Core Design>

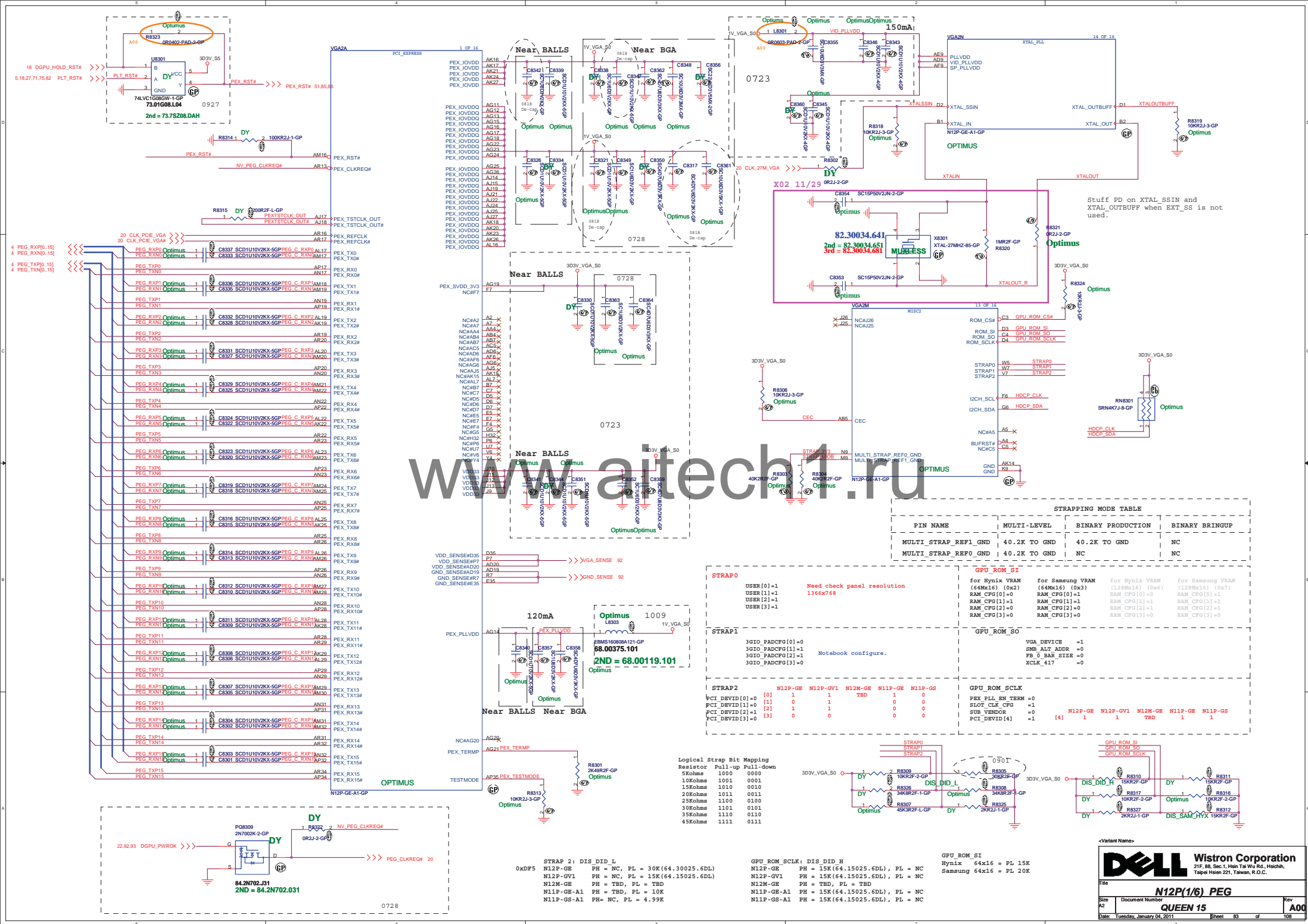


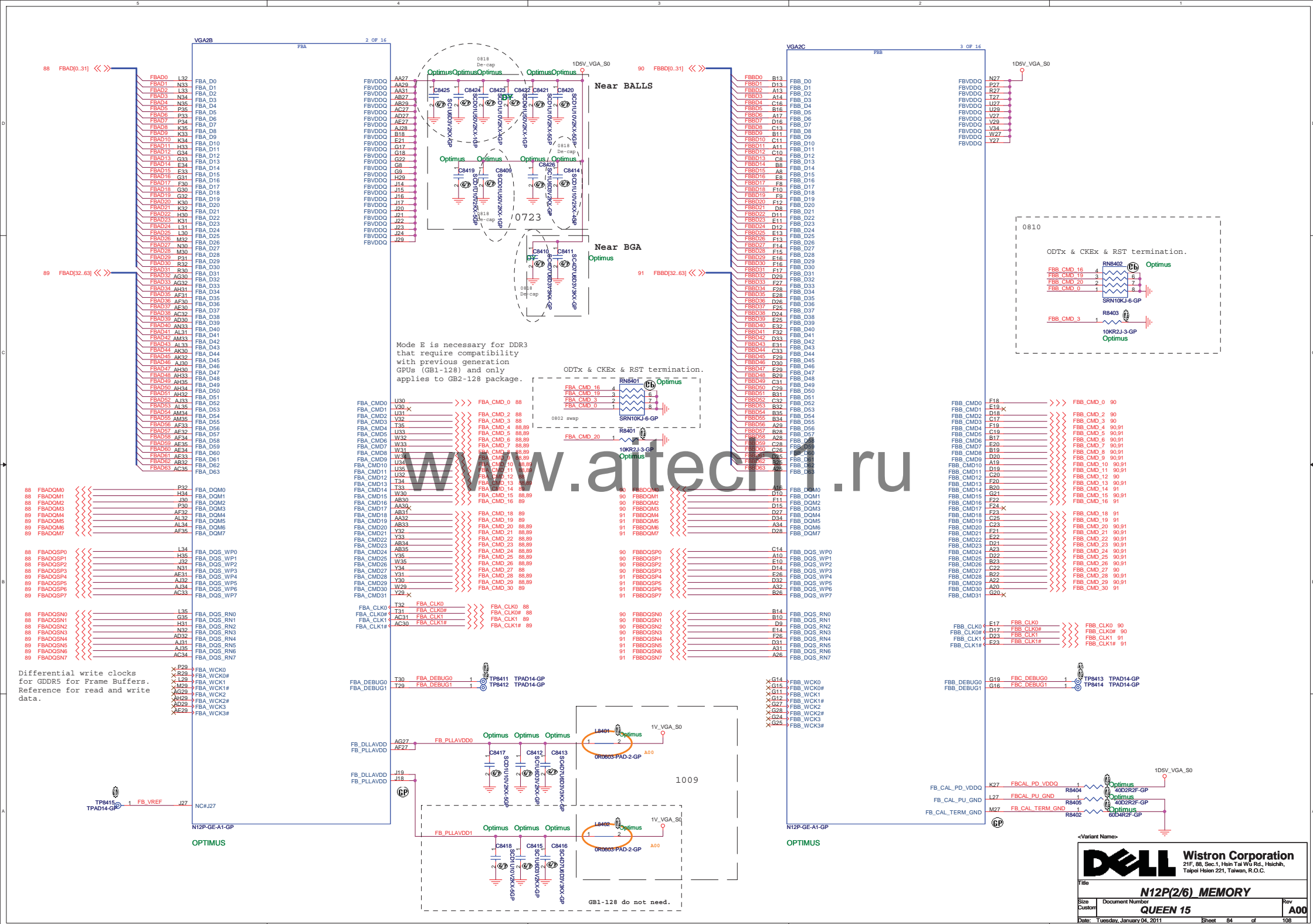
Title
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ent Number  
**QUEEN 15**

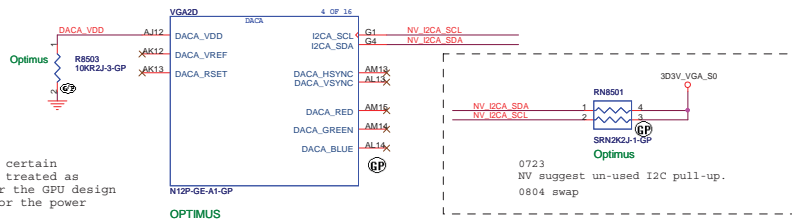
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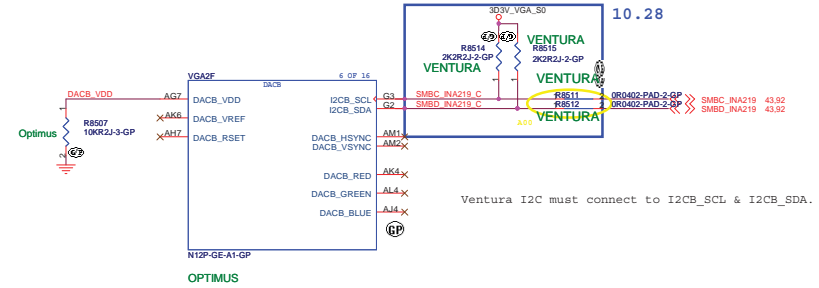


If a DAC interface is not required, it should be disabled by:  
 1. Adding a pull-down to the DACx\_VDD with a 10 kilohm resistor to GND.  
 2. All other DAC I/O pins can be left floating.

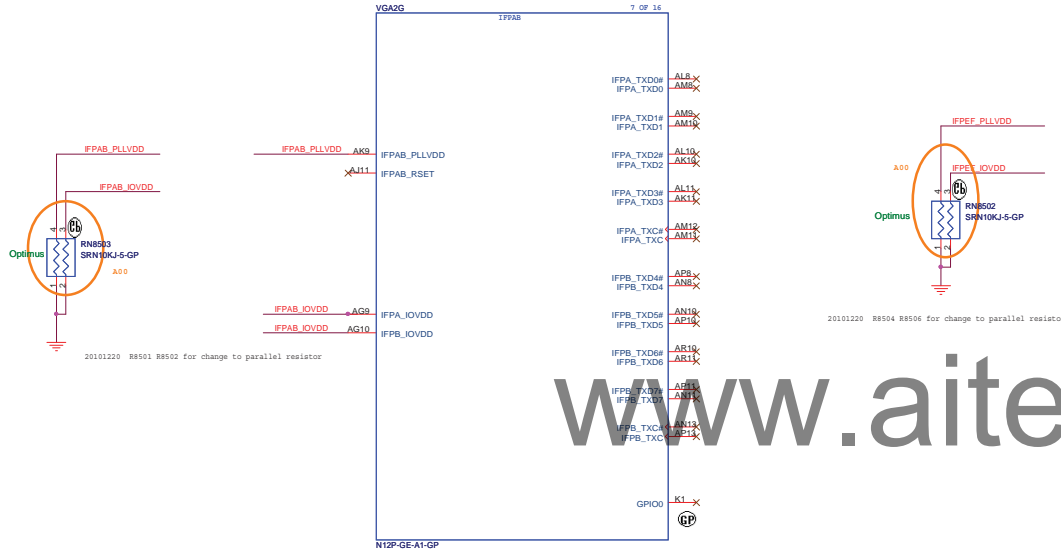


In Optimus mode the GPU does not drive certain interfaces. These interfaces should be treated as unused and appropriate terminations per the GPU design guide should be applied to the signal or the power supply block.

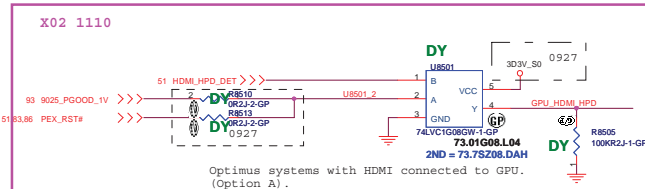
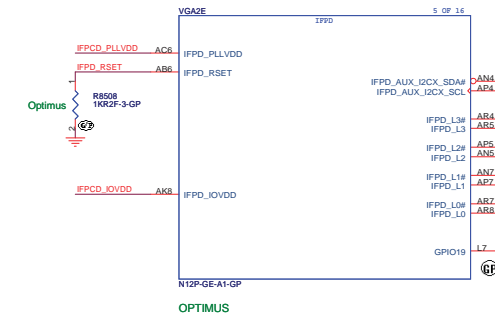
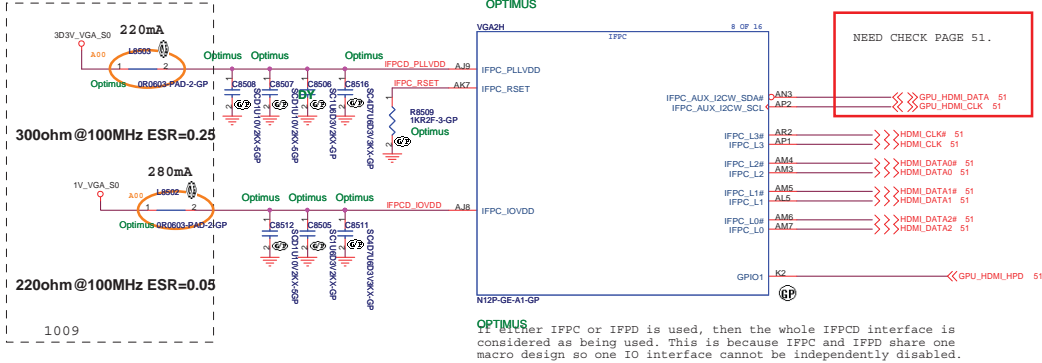
The following guidelines only apply to a fully unused IFP macro:  
 1. Pull down IFPxy\_I0VDD with 10 kilohm resistor.  
 2. Pull down IFPxy\_PLLVDD with 10 kilohm resistor.  
 3. The other IO pins can be NC; this includes unused data lines.

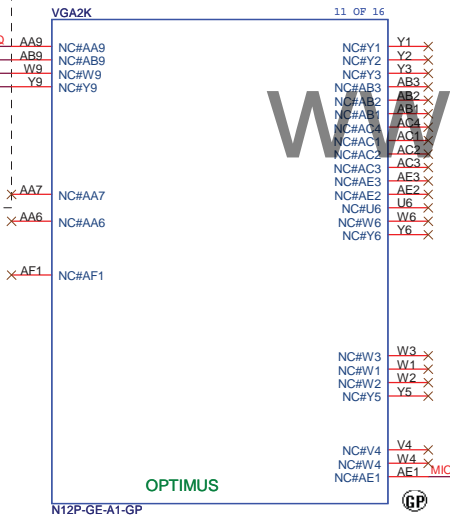
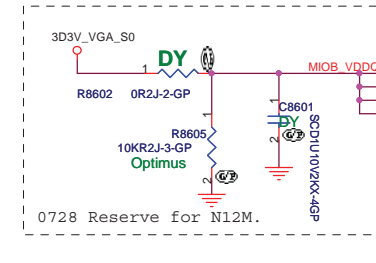
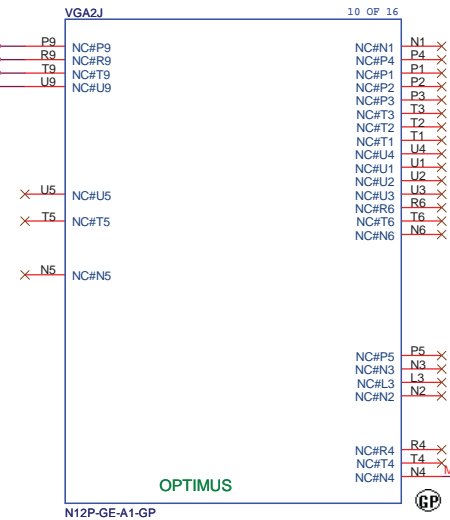
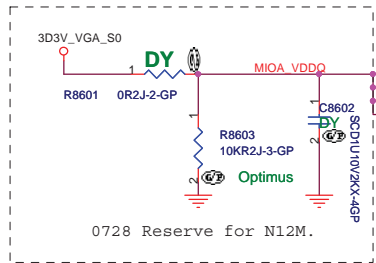


10.28



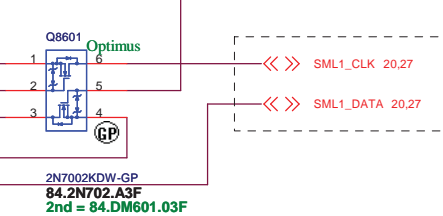
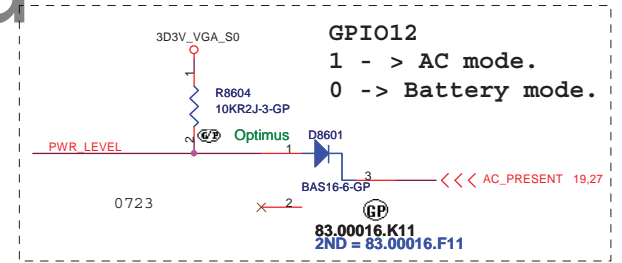
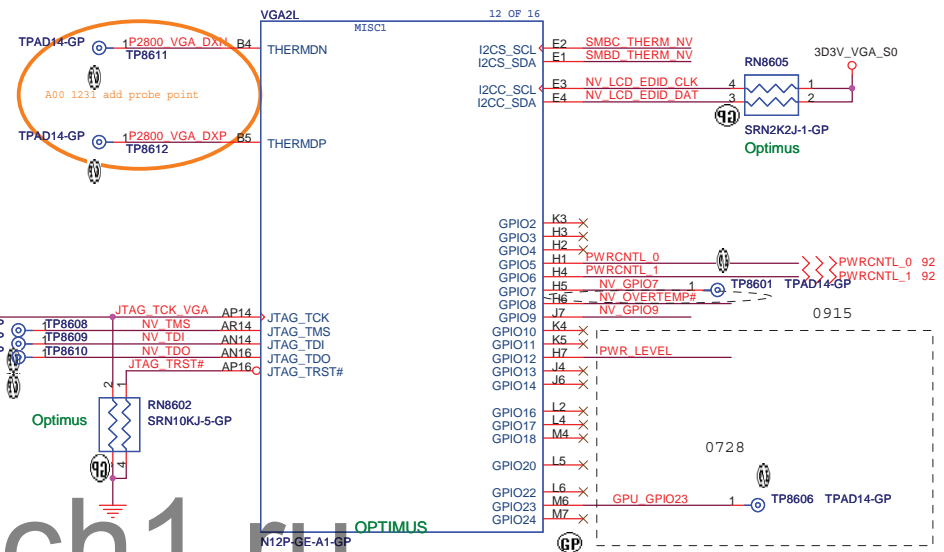
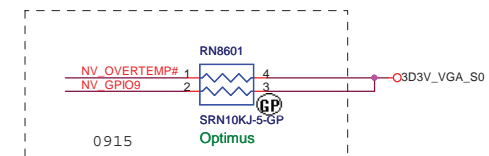
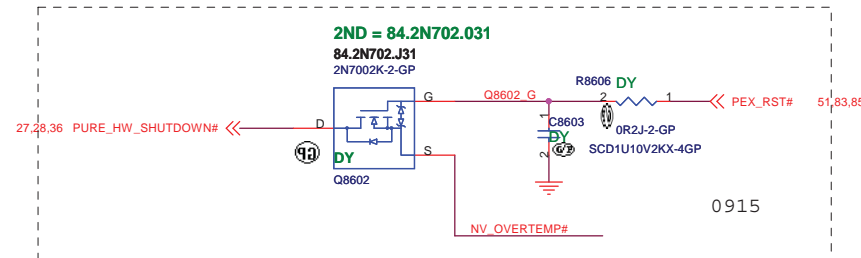
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#### MIOA/B Support

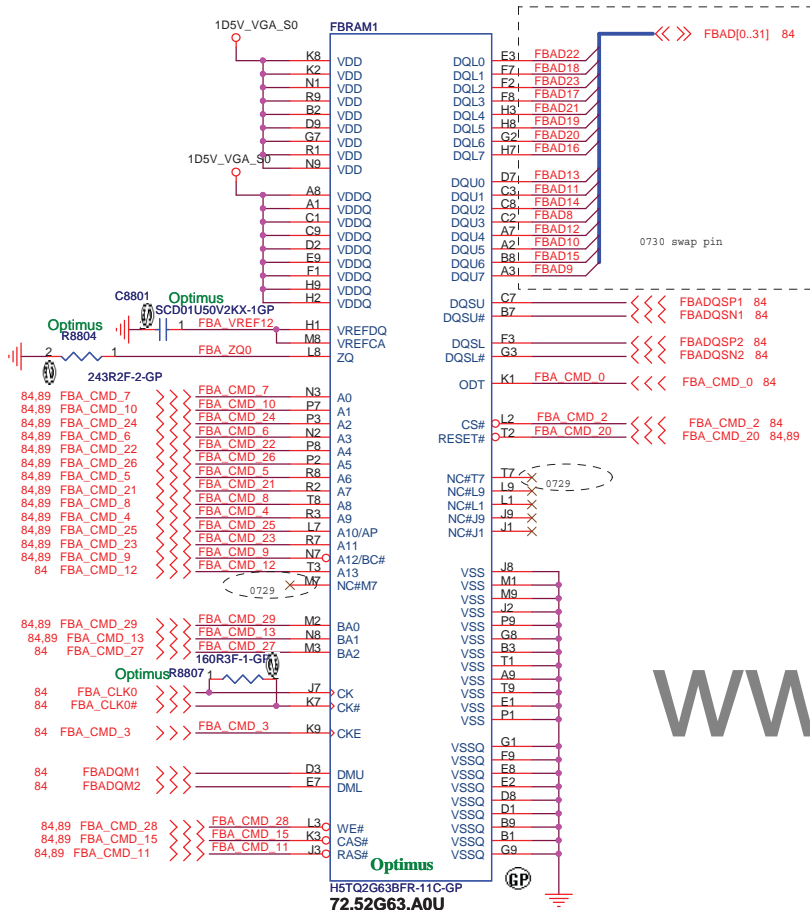
Package	MIOA	MIOB
GB1-192	15-bit, available	TBD
GB2-128	Not available	Not available







# Frame Buffer Partition A Lower 32 bits.

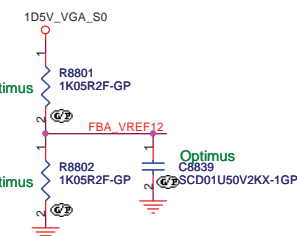


2nd = 72.41164.I0U

PCB Footprint = BGA96D0913H48

1112 X02 Modify:  
All of VRAM PCB footprint change to CO-LAY type  
(DUMMY-BGA96D075133B48) from BGA96D0913H48

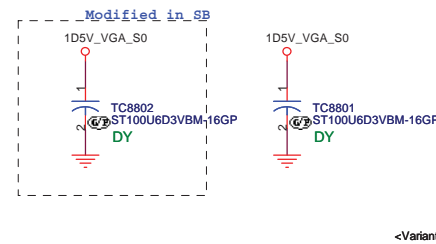
GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function	
CMD25	CMD0	ODT	32.63
CMD23	CMD1	CS1*	
CMD2	CMD2	CS2*	
CMD0	CMD3	CKE	
CMD10	CMD4	A9	A11
CMD8	CMD5	A8	A7
CMD14	CMD6	A3	BA1
CMD7	CMD7	A0	A12
CMD1	CMD8	A8	A8
CMD22	CMD9	A12	A0
CMD20	CMD10	A1	A2
CMD24	CMD11	BA3*	A13
CMD18	CMD12	A13	BA2*
CMD9	CMD13	BA1	A3
CMD28	CMD14	A14	A14
CMD8	CMD15	CAS*	CAS*
CMD27	CMD16	CKE	
CMD19	CMD17	CS1*	
CMD11	CMD18	CS2*	
CMD16	CMD19	ODT	
CMD28	CMD20	RST	
CMD3	CMD21	A7	A6
CMD17	CMD22	A4	A5
CMD5	CMD23	A11	A9
CMD4	CMD24	A2	A1
CMD21	CMD25	A10	WE*
CMD6	CMD26	A5	A4
CMD13	CMD27	BA2	A15
CMD19	CMD28	WE*	A10
CMD12	CMD29	BA0	BA0
CMD30	CMD30	A15	BA2



2nd = 72.41164.I0U

PCB Footprint = BGA96D0913H48

1112 X02 Modify:  
All of VRAM PCB footprint change to CO-LAY type  
(DUMMY-BGA96D075133B48) from BGA96D0913H48



<Variant Name>

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File <b>VRAM(1/4)</b>		
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## D



B

A



1

1

1



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## D



3

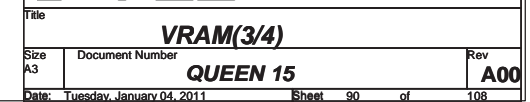
A



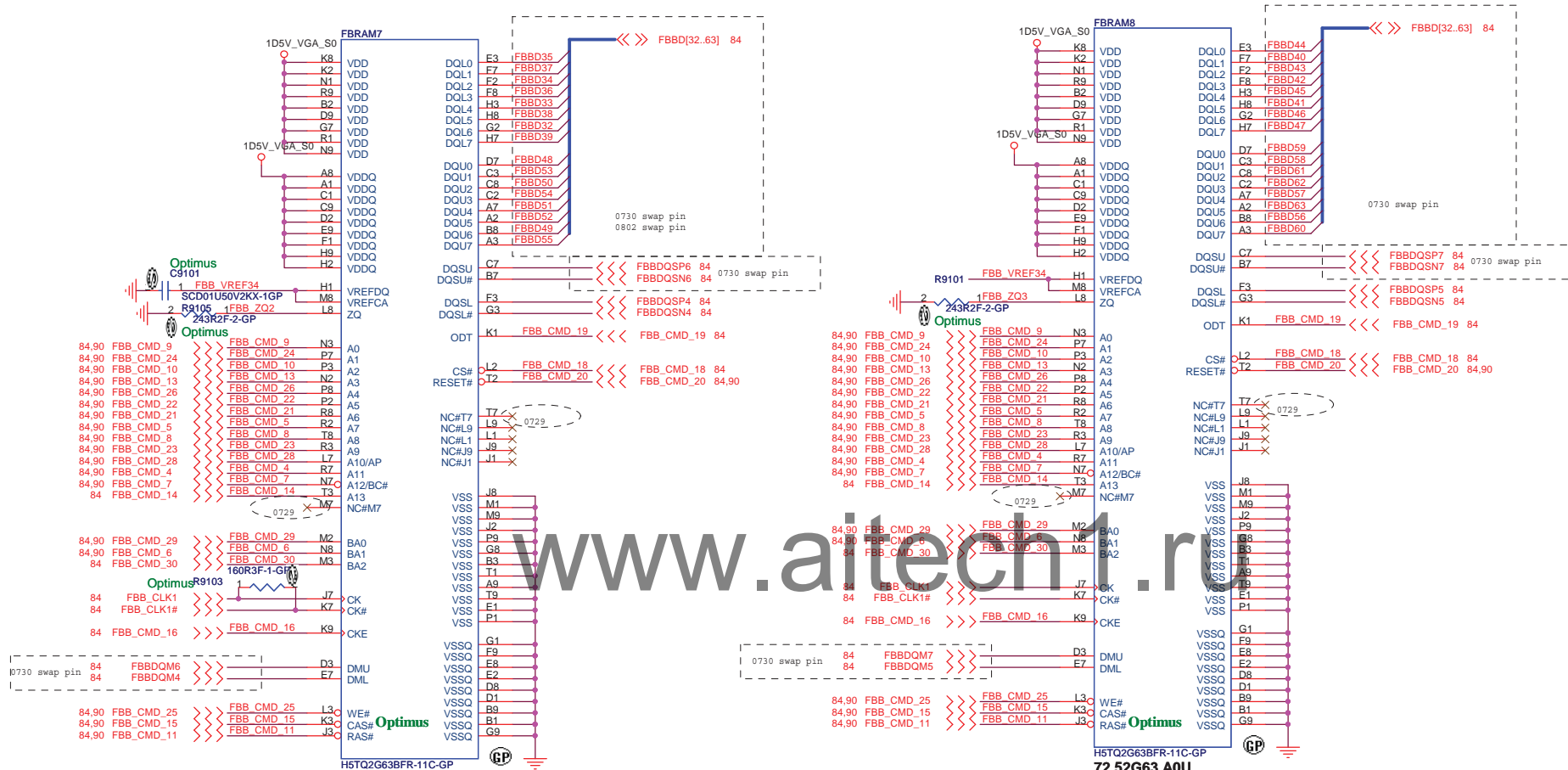
C

8

A



# Frame Buffer Partition B Upper 32 bits.

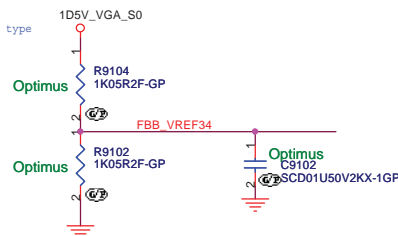


72.52G63.A0U

2nd = 72.41164.I0U

PCB Footprint = BGA96D0913H48

1112 X02 Modify:  
All of VRAM PCB footprint change to CO-LAY type  
(DUMMT-BGA96D075133H48) from BGA96D0913H48



72.52G63.A0U

2nd = 72.41164.I0U

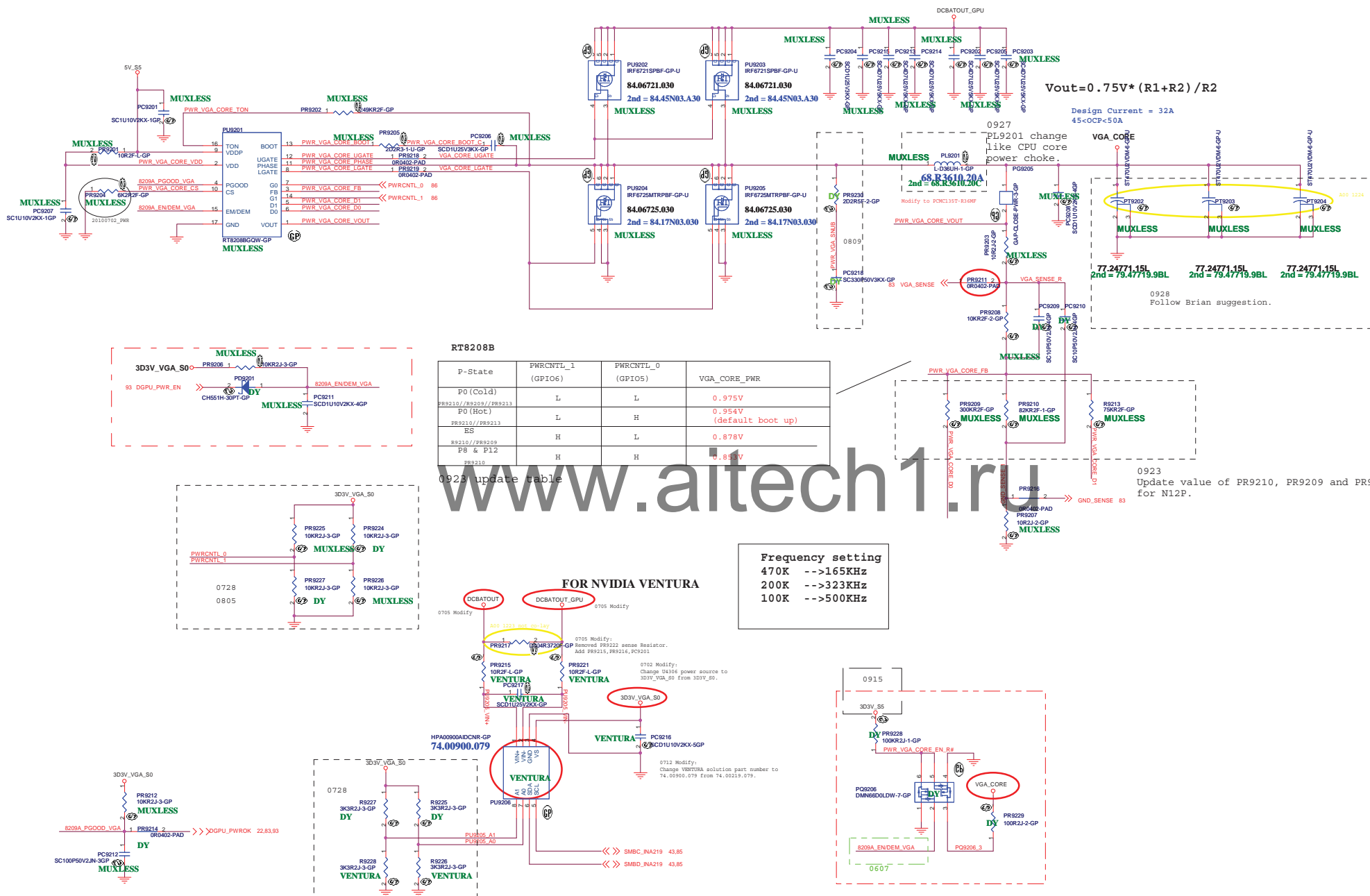
PCB Footprint = BGA96D0913H48

1112 X02 Modify:  
All of VRAM PCB footprint change to CO-LAY type  
(DUMMT-BGA96D075133H48) from BGA96D0913H48

<Variant Name>

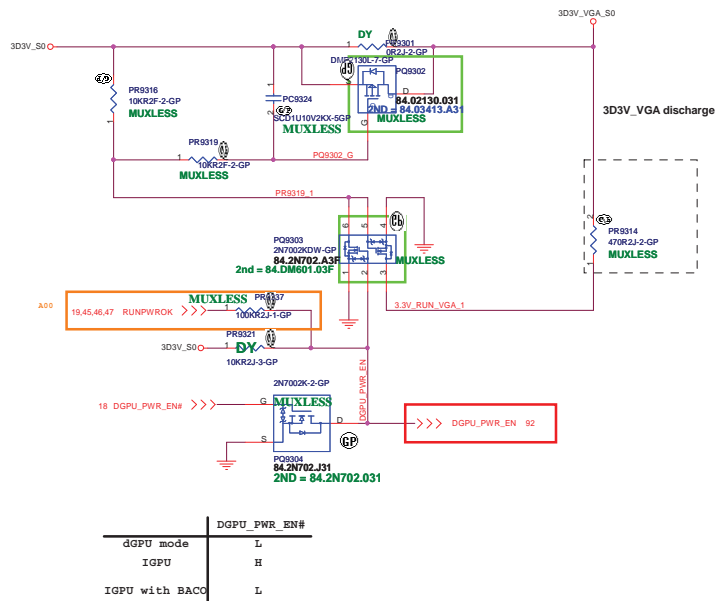
<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: <b>VRAM(4/4)</b>		
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```
SSID = PWR.Plane.Regulator GFX
```



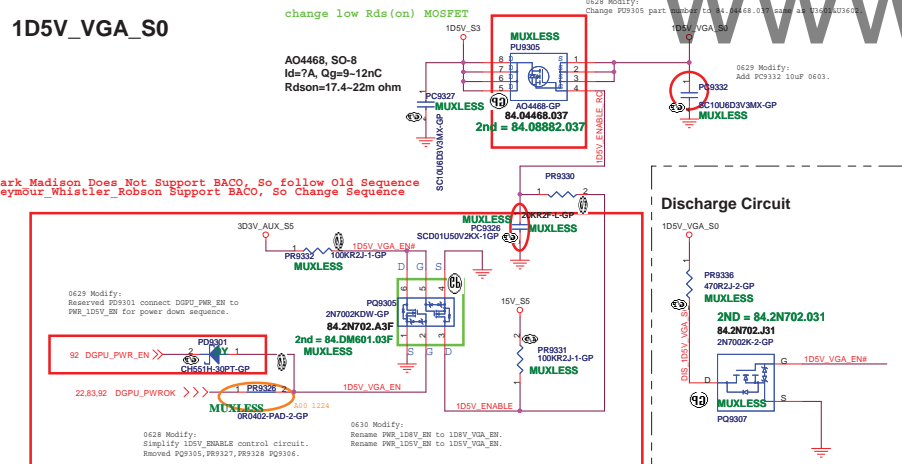
JV10-CS

### 3D3V\_S0 to 3D3V\_VGA\_S0 Transfer

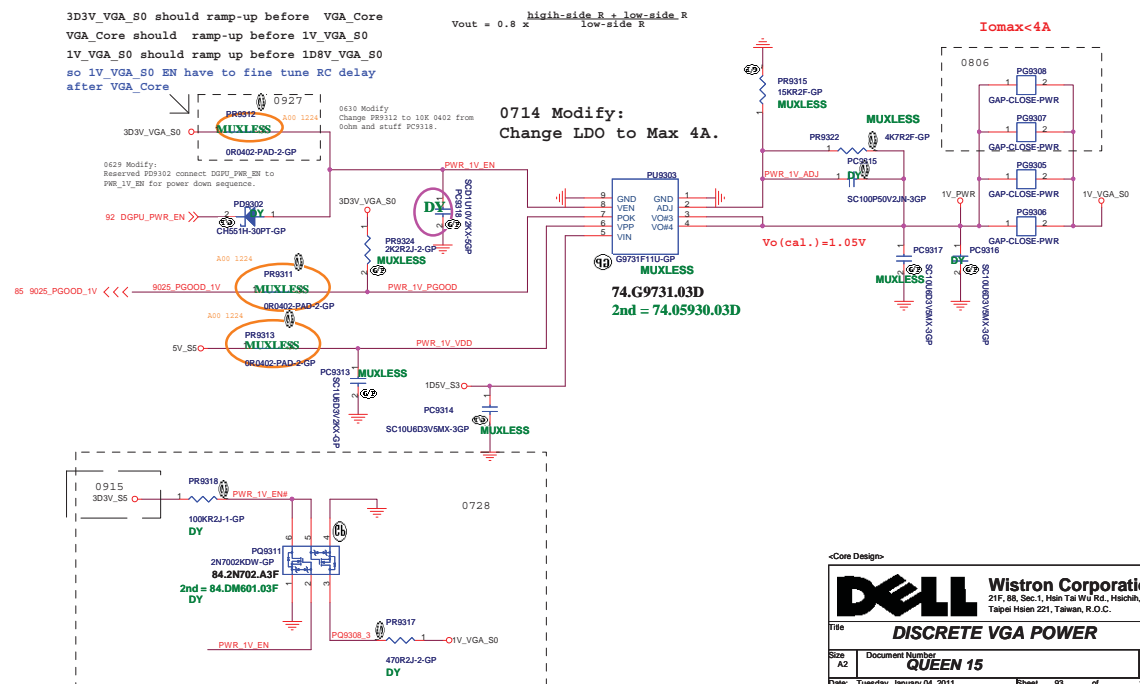


NV do not need 1.8V

**1D5V\_VGA\_S0**




**G9731F11U-GP for 1V S0**



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Title

***LVDS Switch***


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<Variant Name>



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Title

***CRT Switch***

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SSID = SDIO

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<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**TOUCH PANEL**

Size  
A3

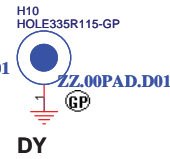
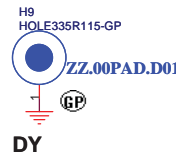
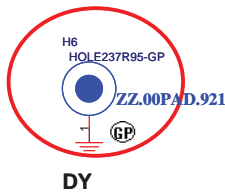
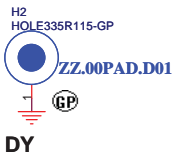
Document Number  
**QUEEN 15**

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**A00**

Date: Tuesday, January 04, 2011

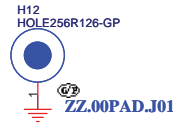
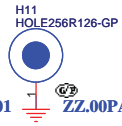
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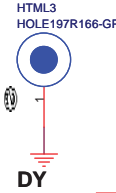
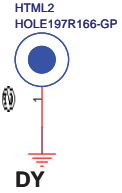
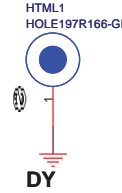


Check test point

0624 Modify:  
Removed AFTP1,AFTP7-AFTP13.

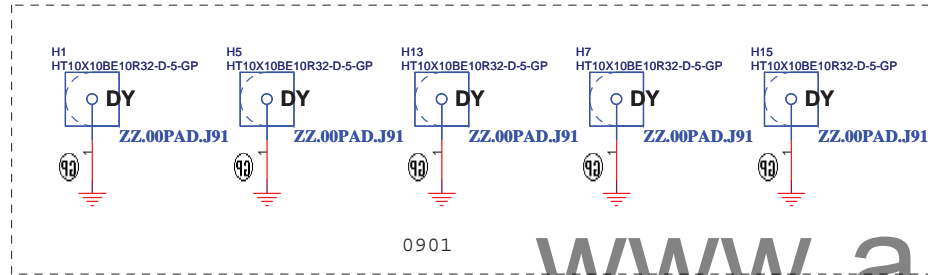


CPU Thermal module hole



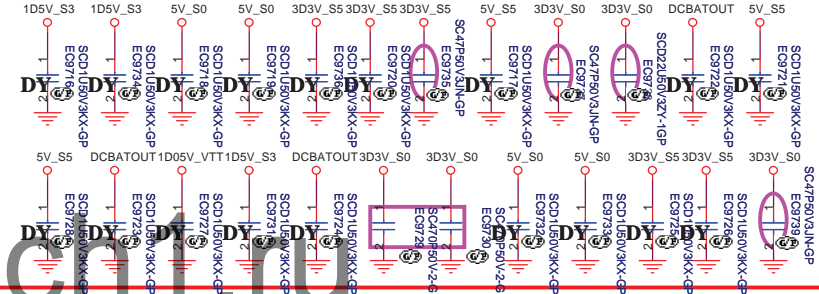
stand off

0721 Modify:  
Removed SPR1

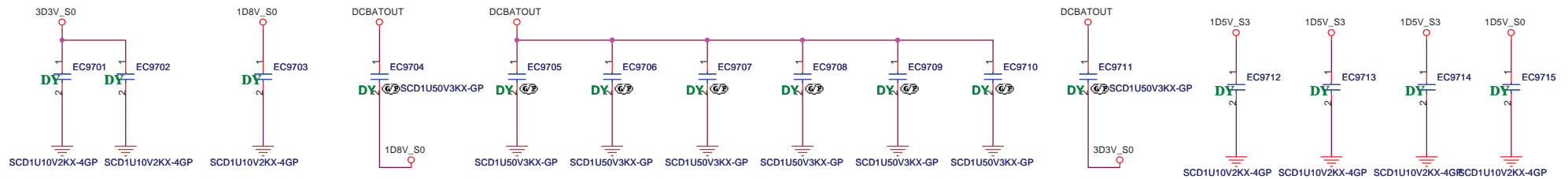


RF CAP

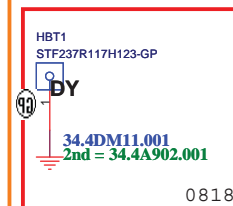
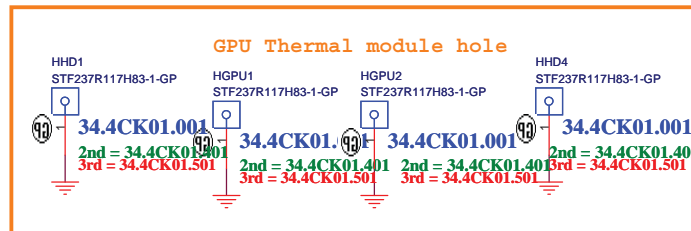
0915 X01 Modify:  
Reserved EC9701-EC9723 0.1uF for  
RP suggestion.



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0802 For EMI/ESD.



0818

<Variant Name>

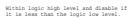


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Title <b>UNUSED PARTS/EMI Capacitors</b>		
Size A3	Document Number <b>QUEEN 15</b>	Rev <b>A00</b>
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(AC mode)

red word: KBC GPIO



VREF\_Sus must be powered up before VocSus\_3, or after VocSus\_3 within 0.7 V. Also, VREF\_Sus must power down after VocSus\_3, or before VocSus\_3 within 0.7 V.

Not floating.

Sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ns de-bounce on the input.

VREF must be powered up before Voc1\_3, or after Voc1\_3 within 0.7 V. Also, VREF must power down after Voc1\_3, or before Voc1\_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

Timing diagram for PCH GPIO54 output. The diagram shows the relationship between several signals during a power-down event:

- GPIO\_PWR\_ENB (Discrete only):** A discrete signal that transitions from high to low, indicated by a dashed line and a transition symbol.
- 3D5V\_VGA\_S0 (VDE33):** A signal that transitions from high to low.
- #2D0A\_EN/#2D5V\_VGA (Discrete only):** A discrete signal that transitions from high to low.
- VGA\_CORE (INVVDI):** A signal that transitions from high to low.
- GPIO\_PWRCK (Discrete only):** A discrete signal that transitions from high to low.
- 1D5V\_VGA\_S0 (FEVDDQ):** A signal that transitions from high to low.

Timing constraints are indicated by arrows and text:

- tINVVDI > 0ms:** The time from the falling edge of #2D0A\_EN/#2D5V\_VGA to the falling edge of VGA\_CORE.
- tFV - FEVDDQ > 0ms:** The time from the falling edge of GPIO\_PWRCK to the falling edge of 1D5V\_VGA\_S0.

Other labels include:

- PCH GPIO54 output:** Located at the top right.
- RT8208 PGOD:** Located on the right side.
- VGA\_CORE 1V, VGA\_S0 1D5V\_VGA\_S0, 3D5V\_VGA\_S0:** Located at the bottom right.
- First rail to power down:** Indicated by a bracket on the left side.
- Last rail to power down:** Indicated by a bracket on the left side.
- tPOWER-OFF < 10ms:** The time from the falling edge of GPIO\_PWR\_ENB to the falling edge of 1D5V\_VGA\_S0.

For power-down, reversing the ramp-up sequence is recommended.

red word: KBC GPIO



VREF\_Bus must be powered up before VccBus1\_3, or after VccBus1\_3 within 0.7 V. Also, VREF\_Bus must power down after VccBus1\_3, or before VccBus1\_3 within 0.7 V.

VS22P must be powered up before Vcc2\_3, or after Vcc2\_3 within 0.7 V. Also, VS22P must power down after Vcc2\_3, or before Vcc2\_3 within 0.7 V.

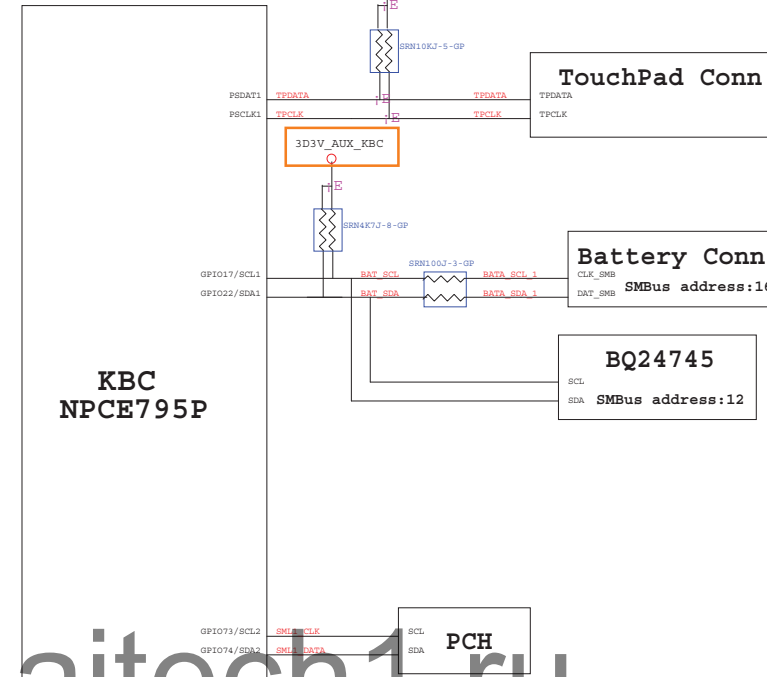
This signal represents the Power Good for all the non-CORR and non-graphics power rails.

[illegible]

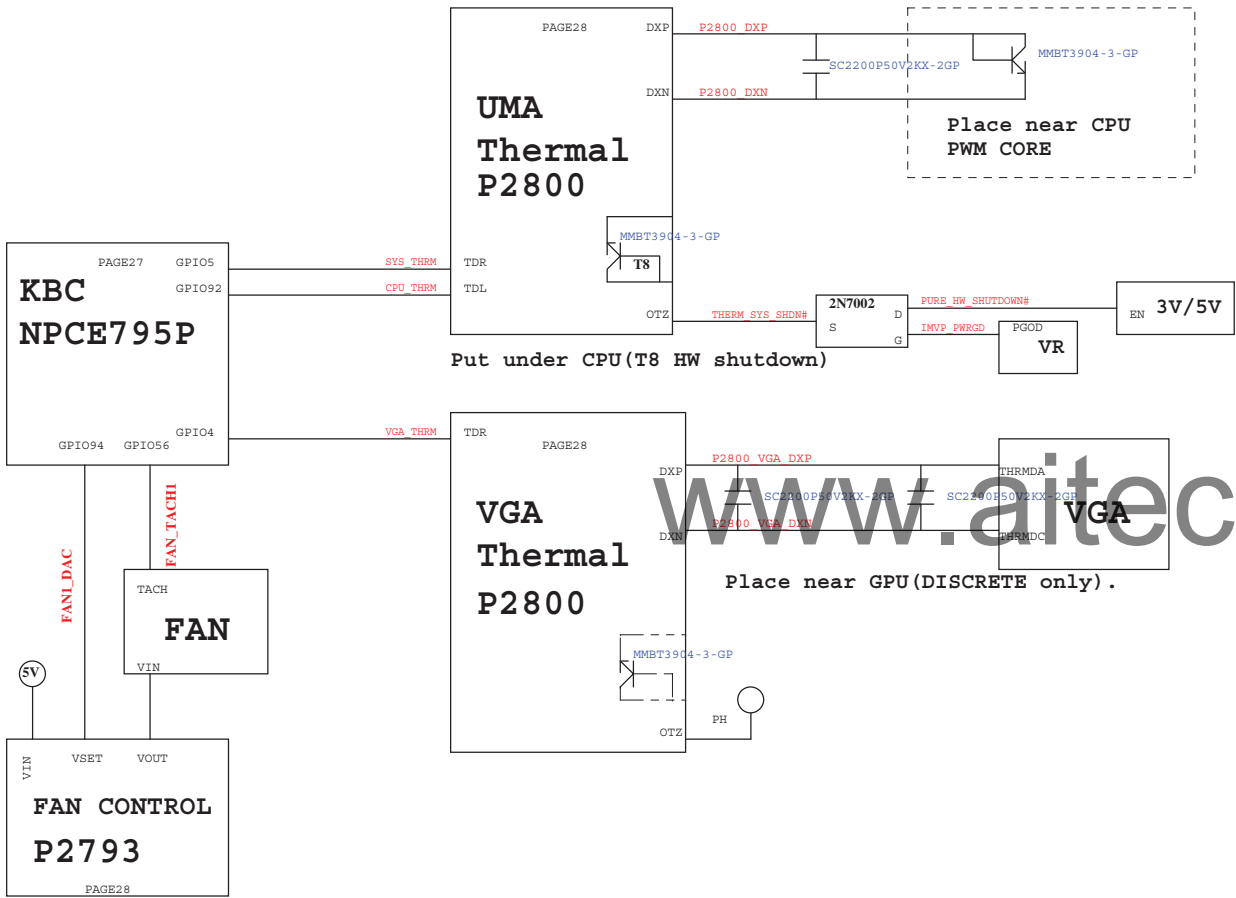
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Title			
<b><i>Power Sequence Diagram</i></b> <b>QUEEN 15</b>			
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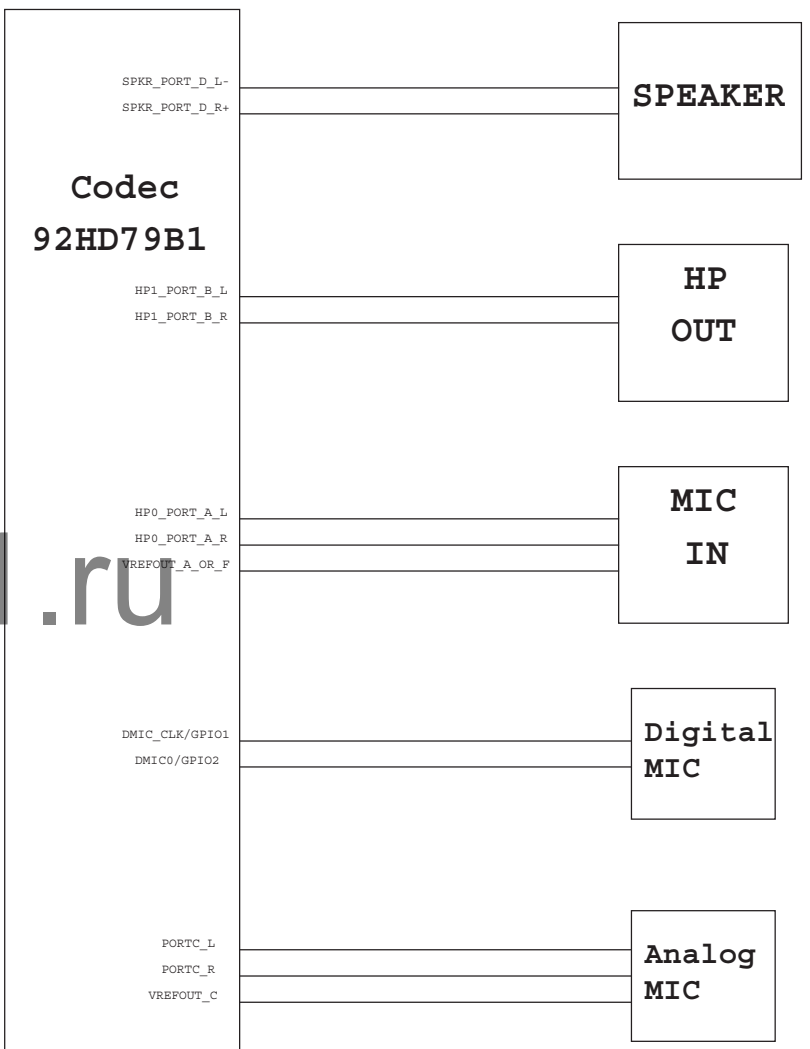
## KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



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VERSION	DATA	PAGE	Change Item
X01	08/25	14	SWAP SA0_DM1 and SA1_DIM1 each other for DM2 can't boot up issue.
	08/29	28	Change U2802 Main source to 74.00991.031, 2nd 74.02793.A31,3rd 74.05606.071
	08/29	61	Add 2nd 77.C1071.20L on TC6101.
	08/29	64	Re-assign FP1 pin define.
	08/29	71	Un-stuff Debug port connector(DB1) on X01.
	08/29	37	Change U3701 pin2 to RUNPWROK from 0D75V_EN. Reserved R3717 0ohm between PM_DRAM_PWRGD and VDDPWARGOOD_R.
	08/29	37	Change R2724 to 20K 0402 from 10K for X01 stage.
	08/29	40	Change 3D3V_AUX_S5 to 3D3V_AUX_KBC to avoid leakage Voltage to 3D3V_AUX_KBC under DC mode.
	08/31	51	HDMI1 change to 22.10296.311 from 22.10296.271
	08/31	28	FAN1 change to 20.F0772.003 from 20.F1639.004
	08/31	57	E-SATA1 change to 22.10321.W11 from 22.10290.141
	09/01	41	PU4104 and PU 4105 horizontally mirror.
	09/01	83	R8305 Change to 30K ohm.
	09/01	97	H1, H5, H13, H7 and H15 change to ZZ.00PAD.J91 from ZZ.00PAD.D01.
	09/01	56	HDD1 add 2nd=62.10065.121.
	09/01	79	U7901 change main source to 74.00351.0B3.
	09/01	42	PR4226 change to 5.62K ohm.
	09/01	45	PTC4502 change to 79.3971V.30L.
	09/03	61	U6101 add 2nd=74.00547.079.
	09/03	49	U4901 add 2nd=74.09724.09F.
	09/03	40	PU4002 and PU4003 add 2nd=84.P1403.B37.
	09/03	24	L2401,L2402,L2403 add 2nd=68.10090.10B.
	09/03	27	DY C2713. Add C2722.
	09/03	47	Add PR4702
	09/03	22	Change FFS_INT2_R from PCH GPIO48 to GPIO15 Removed R2220 and change R2201 default pull up to pull down.
	09/06	20	X2001 add 3rd=82.30020.A31.
	09/06	56	U5601 add 2nd=74.02191.079.
	09/06	93	PU9303 add 2nd=74.05930.03D.
	09/06	37	U3701 add 2nd=73.7SZ08.DAH.
	09/06	23	Add 2nd and 3rd for L2301.
	09/06	23	R434 change name to PR9321. Add PC9324 and PR9319 for soft start.
	09/06	61	TC6101=80.10715.B1L, 2nd=77.C1071.21L, 3rd=77.C1071.20L.
	09/06	56	ODD1 add 2nd and 3rd source. HDD1 add 3rd source.
09/06	49	LCD1 add 2nd source.	
09/06	69	TPAD1 add 2nd.	

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VERSION	DATA	PAGE	Change Item
	09/06	15	DM1 2nd=62.10017.Q31, 3rd=62.10017.K01.
	09/06	14	DM2 2nd=62.10017.P31, 3rd=62.10017.K11.
	09/07	68	Add 2nd source 20.K0343.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/07	69	Add 2nd source 20.K0343.004 on KBLIT1 base on updated connector list.
	09/07	82	Add 2nd source 20.F0085.040 on CRTBD1 base on updated connector list.
	09/07	64	Add 2nd source 20.K0382.006 on FP1 base on updated connector list.
	09/07	75	Add 2nd source 20.K0382.026 on NEW1 base on updated connector list.
	09/07	4-10	Updated CPU1 footprint to SKT-BGA989C470395-1H180 from SKT-BGA989C470395-1H186 base on data base updated. Add 2nd source 62.10040.771 on CPU1 base on updated connector list.
	09/07	75	Change CARD1 to 20.I0129.001 from 62.10051.931 from ME double updated latest DXF&EMN on X01.
	09/07	93	PQ9308 change name to PQ9311.
	09/07	ALL	Change all of single 2N7002 to 84.2N702.J31 from 84.2N702.D31 due to 84.2N702.D31 will EOL.
	09/07	28	Change U2801,U2803 to 74.02800.A71 from 74.02800.071 from vender updated parts. Change R2803&R2817 to 107K from 499K,R2804&R2818 to 226K from 102K base on updated ADJ Table.
	09/08	18, 22	Change FFS_INT2_R from PCH GPIO48 to GPIO14 Keep PCH_GPIO5 PH R2201,PCH_GPIO48 PH R2220. Add R1818.
	09/08	82	1.Rename IOBD1 pin20,22,26,28 to IOBD1_20,22,26,28 from PCIE_TXN5,PCIE_TXP5,PCIE_RXP5,PCIE_RXN5. 2.Add RN8207,RN8208 for optional USB3.0 PCIE or USB2.0 signal.
	09/08	18	Reserved USBP9-USBP10 to IOBD1 pin20,22,26,28.
	09/08	37	Stuff Q3704,R3710; unstuff R3716. U3701 pin2 change to 1.05VTT_PWRGD from RUNPWROK.
	09/08	20	DY R2002.
	09/08	47	Mount PC4710.
	09/08	98	Update N12P power sequence.
	09/09	82	R8201, R8202 and R8203 change to 62 ohm.
	09/10	45	Change PL4501 to 68.2R210.20C from IND-D56UH-27-GP base on Brian updated.
	09/10	41	Change PL4101,PL4102 to 68.2R210.20B from 68.2R210.20Q base on Brian updated.
	09/10	82	Rename IOBD1 pin14 to IOBD1_14 from USB30_SMI#. Add R8207 for USB20 USB_OC#10_11 Add R8206 for USB30 USB30_SMI# Add R8208 for USB20 USB signal. Add R8207 for USB30 PCIE signal.
	09/10	49	Add TPNL1 for touch panel solution 4pin connector. Change LCD1 to 20.F1816.030 for 30pin Re-assign LCD1 pin define base on Roy updated cable pin define list.
	09/10	51	Change HDMI1 part number to 22.10296.331 from 22.10296.311 base on ME Double updated.

VERSION	DATA	PAGE	Change Item
X01	09/13	83	Change X8501 to 82.30034.641;2nd 82.30034.651;3rd 82.30034.681 from sourcer suggestion.
	09/13		Change KBLIT1, PWRBTN2 and TPAD1 2nd source from 20.K0343.004 to 20.K0382.004.
	09/13	47	Change 1.8V power solution.
	09/14	82	Change R8201~R8203 to 470ohm from 100ohm. Add RN8209 PH 5V_S5 on MEDIA_LED1~3# for PWM OD mode.
	09/14	40	Add 2nd source 84.04835.H37 on PU4002,PU4003 base on Brian updated 2nd source excel file.
	09/14	58	Change SPK1 to 20.F0772.004 from 20.F1647.004 from Double updated.
	09/14	51	Add R5101~R5108and reserved TR5101~TR5104 on all of HDMI differential pair for EMC suggestion. Rename HDMI1 CONN NET name.
	09/14	29	Add R2920,R2921 and reserved EC2901,EC2902 on AUD_DMIC_CLK &AUD_DMIC_IN0 for EMC suggestion.
	09/14	75	Add R7503,R7504 and reserved EC7501,EC7502 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion. Rename NEW1 pin24,25 to USB_PP13_R&USB_PN13_R. Rename NEW1 pin8,9 to CLK_PCIE_NEW_C&CLK_PCIE_NEW#_C
	09/14	20	Reserved EC2004,EC2005 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion.
	09/14	49	Reserved EC4910~EC4915 on LVDS signal for EMC suggestion.
	09/15	58	Re-assign SPK1 pin define base on Roy updated excel file for 20.F0772.004
	09/15	51	Add 2nd source 22.10296.311 on HDMI1 from updated connector list.
	09/15	68	Add 2nd source 20.K0382.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	49	Change BLON_OUT_C to pin 15 and pin 4 to NC on LCD1.
	09/15	28, 51,82	Add test point for WKS AFTE request.
	09/15	All	ADD 2nd source follow Power team suggestion.
	09/15	92, 93	Modify PR9318 and PR9228 power source from 3D3V_AUX_S5 to 3D3V_S5.
	09/15	86	Reserve Q8602, C8603 and R8606 for VGA over temp.
	09/15	20	RN2005 swap net.
	09/15	19	RN2005 swap net.
	09/15	48	Change PR4809 to 10K from 100K PH power source change to 3D3V_S0 from S5.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	97	Reserved EC9701~EC9723 0.1uF for RF suggestion.
	09/15	41	Un-stuff PU4101,PD4105,PR4124, PR4125,PR4101 at X01 stage for 5mW issue.
	09/15	69	un-stuff R6907 and stuff R6905,Q6902,R6906 for 5V drive CAP LED.
	09/17	82	Change IOBD1 part number to 20.F1849.080 base on Double updated latest DXF&EMN.
	09/17	49,57 32,64	stuff TR4901 and un-stuff R4911,R4912 at X01 stage from EMC Neo suggestion. stuff TR4902 and un-stuff R4908,R4909 at X01 stage from EMC Neo suggestion. stuff TR5701 and un-stuff R5718,R5719 at X01 stage from EMC Neo suggestion. stuff TR3201 and un-stuff R3211,R3210 at X01 stage from EMC Neo suggestion. stuff TR6401 and un-stuff R6403,R6404 at X01 stage from EMC Neo suggestion.
	09/17	20	Change RN2010~RN2016 to 33ohm from 0ohm from EMC Neo suggestion.
	09/17	37	Change R3710 to 100K from 0ohm to avoid impact 1.05VTT_PWRGD turn off sequence directly.
	09/17	17	Add R1703~R1705 on RGB signal and reserved EC1701~EC1703 0.1u from EMC Neo suggestion.

VERSION	DATA	PAGE	Change Item
X01	09/17	40,41	Stuff EC4002 0.1uF from EMC Neo suggestion. Stuff EC4008 0.1uF from EMC Neo suggestion. Stuff EC4102,EC4103 0.1uF from EMC Neo suggestion. Stuff EC4107 0.1uF from EMC Neo suggestion. Stuff PC4119,PC4120 0.1uF from EMC Neo suggestion. Stuff EC4006,EC4007 0.1uF from EMC Neo suggestion.
	09/17	60,18	EC6001 change to 10p from 4.7p and default stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default stuff from Neo suggestion.
	09/17	44	default stuff EC4407,EC4405,EC4403,EC4410 base on EMC Neo suggestion.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	82	Change R8201~R8203 to 430ohm.
	09/17	48	Change PR4809 to 4.7K from 100K PH power source change to 3D3V_S0 from S5.
	09/17	40,27,83	Rename PCIE_RST# to AD_IA_HW2 on KBC GPIO50 for power Tom suggest. Reserved PQ4004,PR4036,PR4037 for AD_IA_HW2 function.
	09/17	68	Rename CHARGER_LED1 to CHARGERLED1. Rename FPOWER_LED1 to FPOWERLED1. Rename HDD_LED1 to HDDLED1. Rename TP_LOCK_LED1 to TPLOCKLED1. Rename TP_LOCK_LED2 to TPLOCKLED2. Rename WLAN_LED1 to WLANLED1
	09/17	21,22	Base on layout routing,Add RN2104 10K instead of R2111 10K. Move EC_SCI#,DBC_EN to RN2201. Move S_GPIO to RN2103. Move PSW_CLR# to RN2104.
	09/17	56	Change R5605 to 100K from 10K and PH to 5V_S0 from 3D3V_S0 to meet Vgs>2V turn on.
	09/17	56	Add Q2706,Q27002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing.
	09/17	ALL	Change all of 0402 0ohm to 0R0402 short pad. PR4008,PR4010,PR4012,PR4020,PR4023,PR4024,PR4027,PR4028,PR4029,PR4225PR4102,PR4113,PR4118, PR4121,PR4203,PR4204,PR4215,PR4222,PR4231,PR4243,PR4301,PR4509,PR4510,PR4801,PR4804,PR4805, PR4808,PR4810,PR9211  F4902,PR4017,PR4018,PR4106,PR4611,PR4710,PR4807,R2304,R2403,R2406,R2409,R2702,R2902,R2903,R2904 R2305
	09/20	9	Add 2nd for TC901.
	09/20	83	Add 2nd for L8303.
	09/20	82	Add 2nd for LD8201.
	09/20	86	Add 2nd for Q8601.
	09/20	83	Add R8321. C8353 and C8354 change to 12pF.
	09/20	82	Redefine IOBD1.
	09/20	75	AFTP111 and AFTP110 connect to USB_PP13_R and USB_PN13_R.
	09/20	51	Change P/N of Q5102.
	09/21	42	Change PU4201 VDD power source to 5V_S5 from 5V_S0 to avoid abnormal MVP_PWRGD waveform.
	09/21	47	stuff PC4714 22uF from Brian updated.

<Core Design>



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Title

### Change History

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VERSION	DATA	PAGE	Change Item
X01	09/21	45	Change PR4507 to 20K from 20.5K from Brian updated.
	09/21	46	Change PR4602 to 110K from 68K from Brian updated.
	09/21	42	Change PR4217 to 1.27K from 1K from Brian updated. Change PR4213 to 3.6K from 3.16K from Brian updated. Change PR4236 to 3.01K from 3.32K from Brian updated.
	09/21	44	Change PC4410 to 0.01u from 0.022uF from Brian updated.
	09/21	39	Add 2nd 83.00099.K11;3rd 83.00099.T11 on D3901,D3902,D3903 from Sourcer Eden suggestion.
	09/21	39	Add 2nd 84.02143.011;3rd 84.00143.N11 on 6801,Q6804,Q6805,Q6806,Q6807,Q6808 from Sourcer Eden suggestion.
	09/21	43	Change PU4303,PU4306,PU4309 dummy field only for QC CPU stuff. Change PC4307,PC4316 dummy field only for QC CPU stuff. Add 2nd for PTC4306.
	09/21	41	PD4101, PD4103, PD4104 and PD4105 add 2nd source.
	09/21	69	Q6902 add 2nd source.
	09/21	40	PD4001 add 2nd source.
	09/21	19	move PCH_WAKE# to RN1901 pin4;Add R1909 PH 100K on AC_PRESENT.
	09/21	37	R3710 change to 0ohm. Remove R3701 and C3701.
	09/21	42	Add PR4214, PC4230, PR4216 and PC4231 from Brian updated.
	09/23	20	RN2016, RN2010, RN2011, RN2012, RN2014 and RN 2013 keep 0ohm.
	09/23	ALL	PR9216, R504, R1812,R1813,R1815,R1817, R1903, R1906,R1910,R1912,R1913,R1924,R1925, R2213,R2219, R2711,R2720,R2733,R2761, R2807,R2814, R3708, R5125, R5127, R5721, R5722.
	09/23	75	Add R7505~R7508 0ohm and reserved EC7503~EC7506 on PCIE_TX8&RX8 signal base on EMC Lance suggestion. Add R7509,R7510 0ohm and reserved EC7507,EC7508 on CLK_PCIE_NEW_REQ&PCIE_WAKE# signal base on EMC Lance suggestion.
	09/23	ALL	RN5101, RN2201, RN1702, RN1901, RN1705 swap pin.
	09/23	79	DUMMY G-SENSOR.
	09/23	92	Update value of PR9210, PR9209 and PR9213 for N12P.
	09/23	43	PR4320 change to 4 m ohm.
	09/23	68	Add 2nd source 83.00110.J70 on FPOWERLED1,HDDLED1,WLANLED1 from Sourcer Anya suggestion. Add 2nd source 83.00326.G70 on CHARGERLED1from Sourcer Anya suggestion. Add 2nd source 83.00190.Z70 on TPLOCKLED1,TPLOCKLED2 from Sourcer Anya suggestion.
	09/23	69	Change KBLIT1 part number to 20.K0589.004 and re-assign pin define base on Roy updated.
	09/23	42, 44	Add 2nd source 69.60011.201 on PR4405,PR4245 from Sourcer Kitty suggestion.
	09/23	42	Add 2nd source 69.60037.021 on PR4246,PR4247 from Sourcer Kitty suggestion.
	09/24	23	Add 2nd source 68.00214.211 on L2301 updated from DN13ATI.
	09/24	68, 69	Change R6806,R6808,R6811~R6813,R6801,R6803,R6815,R6906 to 390ohm from 1K to fine tune all of MB LED for 5mA spec.
	09/27	51	Reserve R5114 and R5115.
	09/27	85	Reserve R8510 and R8513.
	09/27	83	DY U8301, mount R8323.
	09/27	92	R9206 change to 10K, PC9211 mount 0.1u.
	09/27	93	R9312 change to 1K.

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X01	09/27	49, 57 32, 64	TR4901, TR4902, TR5701, TR3201 and TR6401 DY. Stuff 0 ohm.
	09/27	69	AFTP73 connect to TP_VDD.
	09/27	85	U8501 power change to 3D3V_S0.
	09/27	92	PL9201 change like CPU core power choke.
	09/28	83, 84	L8303, L8401, L8402, L8502 and L8503 follow NV DG spec.
	09/28	46	Change PR4606 to 4.02K from 240ohm for fine tune 1.5V output Voltage.
	09/28	92	PTC9202, PTC9203 and PTC9204 2nd=79.47719.9BL
	09/28	22	Change R2220 to 10K from 100K.
	09/28	60	EC6001 change to 10p from 4.7p and default un-stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default un-stuff from Neo suggestion
	09/28	27	Change R2710, R2739, R2724 and R2726 change to 1%.
	09/29	27	Default mount R2756, Dummy R2734.
	10/04	24	Add 2nd source 68.1001E.10N on L2401,L2402,L2403 from sourcer Renee Lee updated.
	10/07	43	PTC4306 cahnge second source to 79.47612.60L.
	10/09	85	Change L8503 to 68.00375.091,and add second source 68.00206.171
	10/09	85	Change L8502 to 68.00115.191,and add second source 68.00206.131
	10/09	84	Change L8401 and L8402 to 68.00115.181,and add second source 68.00206.341
	10/09	83	Change L8303 to 68.00375.101,and add second source 68.00119.101
	10/09	83	Change L8301 to 68.00115.161,and add second source 68.00206.111
	10/09	42	Change PR4217 to 64.84505.6DL for Dual-core OCP
	10/09	42	Change PR4213 to 64.23715.6DL for Dual-core loadline
	10/09	42	Change PR4207 to 64.22025.6DL for CPU(35W) Turbo setting
	10/09	42	Change PR4202 to 64.22025.6DL for GFX Turbo setting
	10/09	20,83	Dummy R2004 R2003 and PQ8309, stuff R2005
	10/19	28	Change R2817 from 107K to 124K (64.12435.6DL) for VGA temperature setting change
	10/25	84	Change R8402 from 40D2R to 60D4R (64.60R45.6DL) for meeting the spec
	10/25	14 15	Add DM1 and DM2 second source:62.10017.Q41 and 62.10017.P61
X02	10/25	85	Ventura SMBC_INA219_C and SMBD_INA219_C add 3.3V pull high schematic
	11/01	51 85	Change HDMI HPD schematic for cost down
	11/10	27	Change R2724 to 64.33025.6DL for PCB version change
	11/10	83	Change L8301 to 68.00115.181,and add second source 68.00206.341

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X02	11/11	14	DM2 1st change to 62.10017.P61; 2nd change to 62.10017.N41 on ST stage from ME updated connector list.
	11/11	15	DM1 1st change to 62.10017.Q41; 2nd change to 62.10017.N11 on ST stage from ME updated connector list.
	11/11	60	U6001 1st change to 72.25Q32.A01; 2nd change to 72.25320.C01; 3rd change to 72.25P32.C01 on ST stage
	11/11	68	Change CHARGERLED1 2nd to 83.00327.D70 from Sourcer updated.
	11/11	37	Change U3701 1st to 73.7SZ08.EAH;2nd to 73.01G08.L04;3rd to 73.7SZ08.DAH from Sourcer Eason updated.
	11/11	69	Add 2nd 20.K0592.030 on KB1 from ME updated connector list.
	11/11	82	Add 2nd 20.K0465.008 on MEDIA1 from ME updated connector list.
	11/11	58	Add 2nd 20.F1804.004 on SPK1 from ME updated connector list.
	11/11	28	Add 2nd 20.F1841.003 on FAN1 from ME updated connector list.
	11/11	70	Add 2nd 20.F0962.010 on HALL1 from ME updated connector list.
	11/11	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0.
	11/11	60	Add Q6002,R6007 fo FACTORY RTC detect function
	11/11	28	ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.
	11/11	28	Reserved G709T1UF for T8 solution sync with DN13.
	11/12	82	Change R8201, R8202, R8203 from 430 ohm to 1K ohm (63.10234.IDL) for soluting media board LED brightness is too light issue
	11/15	49	Add 2nd 20.F1860.030 on LCD1 from ME updated connector list.
	11/15	8	Reserved C802~C804,C806,C807 10uF 0603 for power team fine tune Vcore quality
	11/15	88 89 90 91	All of VRAM(VRAM1~VRAM8) PCB footprint change to CO-LAY type (DUMMY-BGA96D075133H48) from BGA96D0913H48 same as DW30.
	11/15	68 69	Change R6813, R6906 from 390 ohm to 1K ohm (63.10234.IDL) for soluting LED brightness is too light issue
	11/15	20	Dell required us to disable PCIE port of WWAN slot ,If PCIE port 1 is disabled, it will cause all PCIE port disabled,so change WWAN to PCIE port 3 from port1 at ST stage.
	11/16	97	Change HHD1 HDD4 HGPU1 HGPU2 2nd from 34.4CK01.201 to 34.4CK01.401 from ME update connector list
	11/16	68	Change R6808, R6811 from 390 ohm to 1K ohm (64.10234.IDL) for soluting LED brightness is too light issue
	11/16	28	stuff both G709T1UF and P2800 related circuit, add R2805 0ohm default un-stuff at ST stage.
	11/17	48	CO-LAY APL5916 related circuit for VCCSA LDO solution.
	11/18	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2301 and un-stuff L2301.
	11/18	28	Add R2805 0hm between THERM_SYS_SHDN#_ OTZ and THERM_SYS_SHDN#. Add R2812 0ohm between THERM_SYS_SHDN# and U2805 pin3.

VERSION	DATA	PAGE	Change Item
X02	11/18	28	Rename U2801&U2804 pin 8 to THERM_SYS_SHDN#_ OTZ from HERM_SYS_SHDN#.
	11/18	20	Change X2001 to 82.30020.D41 from 82.30020.851 from Sourcer Dick updated.
	11/18	23	Reserved R2308,R2309 on VCCVRM power rail.Reserved U2302 LDO circuit on VCCVRM power rail
	11/18	22 82	Rename USB3_PWR_ON to PCH_GPIO57. Add R8209,R8210 for PM_SLP_S4# and VGA_THRM to control USB3_PWR_ON
	11/18	48	Change PTC4801 to 100u(77.21071.07L) from 150u from power team Brian updated
	11/19	74	Add 2nd 20.I0135.001 on CARD1 from ME updated connector list.
	11/19	82	Add 2nd 20.F1908.080 on IOBD1 from ME updated connector list.
	11/20	3	Updated PCIE ROUTING
	11/20	28	Change U2801,U2804,U2805 VCC power to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2812, un-stuff R2805
	11/20	23	Reserved R2308 on VCCVRM power rail. Reserved U2302 LDO circuit on VCCVRM power rail.
	11/20	48	Set TPS51461 PWM solution dummy field for VCCSA_PWM and APL5916 LDO solution dummy field for VCCSA_LDO. default stuff VCCSA_LDO at ST stage
	11/20	22	Rename GFX_CRB_DET to GSENSOR_DET on GPIO39.
	11/20	60	Un-stuff R6007 10M.
	11/20	82	Reserved EC8201~EC8202 0.1u(closed H3) between AGND and GND from EMC Neo suggestion.
	11/20	82	Reserved EC8203~EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/20	82	Add RN8205 base on HSYNC&VSYNC report
	11/20	61	Removed R6101 and connect USB_PWR_EN# to U6101 pin4 directly.
	11/20	22	Rename PCH_GPIO12 to RTC_DET# on GPIO12.
	11/20	61 22 18	Reserved U6102 USB POWER related circuit to separate EATA and CRT USB power in ST build. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/20	82	Reserved R8211,R8212 0ohm 0805 on CRTBD1 pin37,39 to separate EATA and CRT USB power in ST build.
	11/22	82	Swap RN8205 pin4,3 and pin2,1 each other base on Connie swap report.
	11/22	82	stuff EC8201,EC8202 0.1u(closed H3) between GND and GND from EMC Neo suggestion. stuff EC8206 between 3D3V_S5 and GND from EMC Neo suggestion.
	11/22	23	base on layout condition change 3D3V_DAC_S0 circuit. Stuff R2301 and un-stuff L2301.
	11/22	82	stuff EC8203~EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/22	23	Removed U2302 LDO for VCCVRM.

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X02	11/22	29	change R2920,R2921 to 22ohm from 0ohm and stuff EC2901,EC2902 22p from EMC Neo updated.
	11/22	61	Change U6101 to dual USB power switch from single for Layout limitation and placement. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/22	49	stuff C4908 0.1uF from EMC Neo suggestion.
	11/22	57	Change TR5701 to 69.10103.041 and un-stuff R5718,R5719 from EMC Neo Suggestion.
	11/22	49	Change TR4902 CM choke to 69.10103.041 and un-stuff R4908,R4909 from EMC Neo Suggestion.
	11/22	49	Swap TR4901 pin4,3 and pin2,1 each other base on Connie swap report. Change TR4901 CM choke to 69.10103.041 and un-stuff R4911,R4912 from EMC Neo Suggestion.
	11/22	75	Change TR7501 CM choke to 69.10103.041 and un-stuff R7501,R7502 from EMC Neo Suggestion.
	11/22	58	stuff EC5801~EC5804 470pF from EMC Neo suggestion.
	11/22	9 39 45 49	stuff EC901, EC3903, EC4501, EC4909, EC4907 0.1uF from EMC Neo suggestion.
	11/22	49	Change RN4901 to 100ohm 4p from 8p for improve layout place.
	11/22	48	Updated VCCSA_LDO circuit from Power team Brian updated.
	11/22	83 84 85	Change L8301 L8401 L8402 to 0 ohm resistor (63.00000.00L)
	11/22	60	stuff R6007 10M.
	11/23	49 57 75	SWAPTR4901 TR4902 TR5701 TR7501 pin1&4 and pin2&3 each other base on Connie swap report.
	11/23	60	Change U6101 1st(74.02182.071);2nd(74.00546.A7D);3rd(74.02062.079) from Sourcer Harrison suggestion.
	11/23	64	Add C6402 0.1uF,C6403 180pF and stuff C6401 47pF from RF fine tune result.
	11/23	57 49 75	Change R5718,R5719,R4908,R4909,4911,R4912,R7501,R7502 to 0ohm 0603 from 0402.
	11/23	56 97	stuff EC9739,EC9737,EC9735 47pF from RF fine tune result. stuff EC5601 180pF from RF fine tune result. Stuff EC9738 0.22uF closed EC9739 from RF fine tune result.
	11/23	97	stuff ECEC9729,EC9730 470pF from EMC Neo suggestion.
	11/23	45	Change PR4501 to 75K from 45.3K for 1.05V OCP set to 20A from Brian.
	11/23	82	Removed R8211,R8212 and connect 5V_USB2_S3 to CRTBD1 pin 37 directly.
	11/23	61	Removed C6105,C6103.
	11/23	69 70	Change AFTP 80 81 to AFTP 83 84; change AFTP 83 to AFTP82; change AFTP 82 to AFTP85.
	11/24	20	Add 2nd(82.30020.G71);3rd(82.30020.G61) on X2001 from Sourcer Dick updated.
	11/24	69	Add 2nd(20.K0613.004)on KBLIT1 from Karl updated.

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X02	11/24	57	Add 2nd(22.10339.261)on ESATA1 from Karl updated.
	11/24	28	un-stuff VGA P2800 related circuit from Niki confirmed.
	11/24	64	rename C6401,C6402,C6403 to EC6401,EC6402,EC6403
	11/24	22	Dummy R2206
	11/25	28	Dummy R2817 R2818 C2816
	11/25	69	Add 3rd(83.00110.R70) on FPOWERLED1,HDDLED1,WLANLED1 from Anya provide
	11/25	69	Add 3rd(83.00192.J70) on TPLOCKLED1 and TPLOCKLED2 from Anya provide.
	11/25	69	Add 3rd(83.01108.070) on CHARGERLED1 from Anya provide.
	11/26	43 92	Change PC9217 PC4319 to 0.1u 50V
	11/29	83	Change C8353 C8354 to 15PF ,R8320 stuff from vendor suggestion.
	11/29	36	Stuff D3602
	11/30	68	Change 2nd source to 83.00322.070 from 83.00110.J70
	11/30	85	Change L8502 L8503 to 0 ohm
	11/30	92	Stuff PR9237 DY PR9321
A00	12/01	8	Change C807,C826 to 22uF from 10uF and default stuff from Power Brian updated.
	12/01	8	Change C801~C807 and C817 10uF stuff at QC CONFIG from power Brian updated.
	12/21	ALL	Change 0402 pad(ZZ.00PAD.M11): R1404 R1405 R1503 R1504 R1703 R1704 R1705 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R2762 R3614 R3710 R5114 R5801 R5802 R5803 R5804 R8210 R8323 R8511 R8512
	12/21	82	Change 0603 pad(ZZ.00PAD.M21): R8206 R8207
	12/21	17 20	Change resistor pad(ZZ.0R04P.ZZZ): RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2015 RN2016
	12/21	83 84 85	Change L8301, L8401,L8402,L8502,L8503 to 0R0603 pad(ZZ.00PAD.M21)
	12/21	ALL	Change to Parallel resistor R1501 ,R1502; R2739 ,R2774;R8202 ,R8203;R8501 ,R8502;R8506 ,R8507;R2123 ,R2124
	12/21	82	RN8205 change to R8201, R8202
	12/21	93	PR9237 rename to PR9337
	12/21	56 61 68	Delete 77.C1071.21L(TC6101), delete 83.01108.070(CHARGERLED) , delete 62.10065.121(HDD1)

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A00	12/22	27	R2724 change to 47K resistor for XBuild
	12/22	27	R2301 change to 0 resistor for CRT debug
	12/22	40	1.Change PR4032,PR4034,PR4037 to ZZ.00PAD.M11 2.Stuff PQ4003,PQ4004 3.Change PR4047 to 174K(64.17435.6DL) 4.Change PR4035 to 300K(64.30035.6DL) 5.Change PR4036 to 76.8K(64.76825.6DL) 6.Change PR4031 to 150K(64.15035.6DL)
	12/23	68	1.FPOWERLED1 rename to FPLED1 2.HDDLED1 rename to HDLED1 3.CHARGERLED1 renamtpe to CHLED1 4.WLANLED1 rename to WLED1 5.TPLOCKLED2 rename to TPLED2 6.TPLOCKLED1 rename to TPLED1 7.PWRBTN1 rename to PWRBT1 8.PWRBTN2 rename to PWRBT2
	12/23	43	Delete PR4323,PR4324,PR4325; Stuff PR4320 for all BOM ,not co-lay Ventura
	12/23	92	Delete PR9220,PR9222,PR9223; Stuff PR9217 for all BOM ,not co-lay Ventura
	12/23	51	Change 5V_HDMI to 5V_CRT_S0_R for HDMI power leakage
	12/24	All	PRN3901 rename to PN3901 PTC9202-04 rename to PT9202-04 PTC4301-04 rename to PT4301-04 PTC4306 rename to PT4306 PTC4308-09 rename to PT4308-09 PTC4401-03 rename to PT4401-03 PTC4502 rename to PT4502 PTC4602 rename to PT4602 PTC4102 rename to PT4102 PTC4104 rename to PT4104
	12/24	28	Change U2802 3rdto 74.05606.A71 at X-Build batch run
	12/24	82	Change RN8205 to 66.22036.04L from 66.22036.040at X-Build stage
	12/24	82	Reserved R8211 0603 0ohm on F8201
	12/24	36	Reserved Q3603 2N702 on IMVP_PWRGD to fine tune glitch waveform when AC lose and DC lose.
	12/24	28	Change 3D3V_S0 to 3D3V_DAC_S0
	12/24	45 46 93	Change to short pad: PR4502,PR4607,PR9311,PR9312,PR9326. DUMMY PC4501
	12/27	28	If stuff P2800EA1 then must stuff R2803,R2804,C2805 but if stuff P28003B0 should be unstuff.
	12/27	42	PR4207,PR4213,PR4217 DUMMY field set to DC&QC option
	12/28	51	Change 5V_HDMI to 5V_CRT_S0_R on RN5101
	12/28	28	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at XBuild

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A00	12/28	27	Change R2756, R2763, R2766 to short pad
	12/28	36	Stuff Q3603
	12/28	28 86	Cancel VGA Thermal sensor P2800 circuit
	12/28	27 28 82	Change to VGA_THRM to USB3_PWR_ON
	12/28	23	Change R2301 to short pad
	12/29	51	Change HDMI resistor to short pad
	12/29	49,57,75	Delete USB DUMMY resistor for no-lay
	12/29	32	Change USB 0 resistor to short pad for no-lay
	12/29	5	Reserve EC502 ,EC504 for EMI suggestion,add DUMMY EC505 for EMI
	12/29	82	Delete PM_SLP_S4# line, directly link to USB3_PWR_ON
	12/29	23	Add 3rd Richtek(74.09198.G7F) on U2301 at XBuild batch run config
	12/29	68	Not use Liteon LED(83.00322.070) for package
	12/30	5	Add DUMMY diode EC506 for BUF_CPU_RST# as EMI suggestion
	12/30	41	PC4227 change to 78.33420.5FL as 78.33423.5FL obsoleted
	12/30	49	Change R4904 to short pad
	12/31	86	Add probe point for P2800_VGA_DNX/P2800_VGA_DXP
	01/03	68	Change TPLED1,2 1st to 83.01921.P70 ,2nd to 83.00190.S7A,3rd to 83.00191.H70; R6813 change to 390R from 1K same as DN13 LED part.
	01/03	49	Delete R4908, R4909 for USB_Camera not co-lay
	01/03	4-10	Add 3rd foxconn(62.10055.321) on CPU1 at X-Build batch run config
	01/03	82	Add 3rd T-conn(20.F1932.040) on CRTDB1at X-Build batch run config
	01/03	97	Add 3rd LIDON(34.4CK01.501) on HHD1,HHD4,HGPU1,HGPU2 at X-Build batch run config
	01/04	68	Delete 83.00191.H70 for TPLED1,2 as cost high
	01/04	49,57,75	Add 2nd TAI-TECH(69.10084.071) on TR4901,TR4902,TR5701,TR7501 at X-Build batch run config

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